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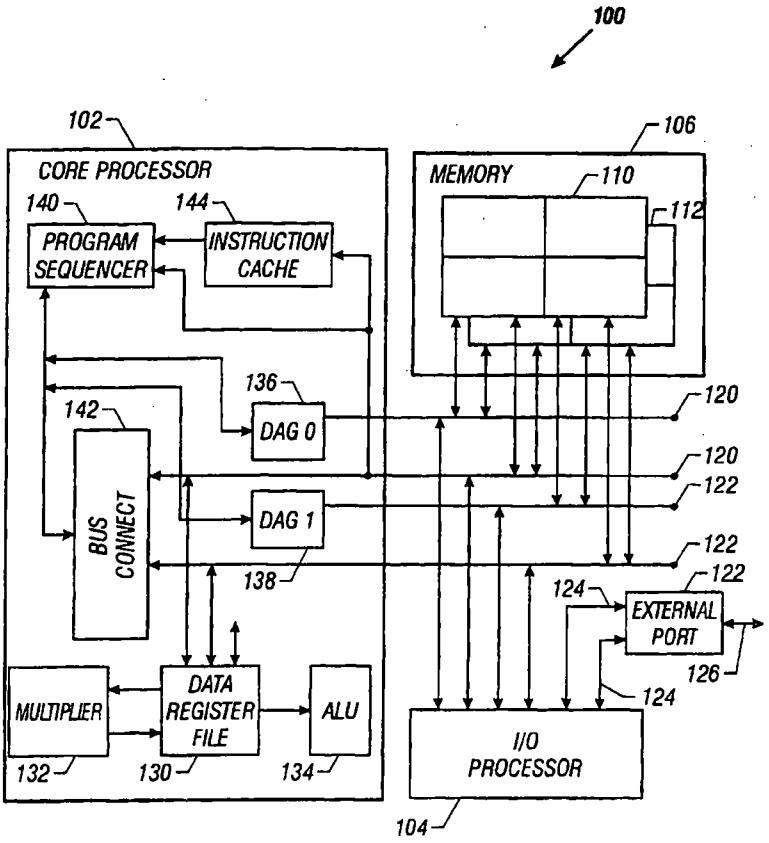
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[Continued on next page]

(54) Title: SYSTEM HAVING A CONFIGURABLE CACHE/SRAM MEMORY

(57) Abstract: An apparatus having a core processor and a memory system is disclosed. The core processor includes at least one data port. The memory system is connected in such a way as to provide substantially simultaneous data accesses through the data port. The memory system can be made user configurable to provide appropriate memory model.



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