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(54) STATIC INDUCTION TRANSISTOR AND A METHOD OF MAKING THE SAME

(71) We, KABUSHIKI KAISHA DAINI SEIKOSHA, a Japanese Company of 31-1, 6-chome, Kameido, Koto-ku, Tokyo, Japan, do hereby declare the invention for which we pray that a patent may be granted to us and the method by which it is to be performed to be particularly described in and by the following statement:—

This invention relates to static induction transistor and to methods of making the same.

According to the present invention there is provided a static induction transistor having a drain region, a source region; a gate region; a channel region surrounded by the gate region, and an impurity region of the same conductivity type as the gate region the impurity region extending completely across the channel region and being disposed between and spaced from the drain region and the source region.

The gate region and the said impurity region may be of P conductivity type material.

Preferably the drain region is surrounded by the gate region.

According to a further aspect of the present invention there is provided an inverter including a static induction transistor as recited above.

According to a yet further aspect of the present invention there is provided a method of making a static induction transistor having a drain region; a source region; a gate region; and a channel region surrounded by the gate region including forming an impurity region of the same conductivity type as the gate region the impurity region extending completely across the channel region and being disposed between and spaced from the drain region and the source region.

In the preferred embodiment a first part of an epitaxial layer is grown on a substrate, the said impurity region is formed in the said first part of the epitaxial layer, and the second part of the epitaxial layer is then

grown and the gate region and the drain region are then formed in the second part of the epitaxial layer. 50

The invention is illustrated, merely by way of example, in the accompanying drawings, in which:—

Figure 1 is an equivalent circuit diagram of a two-stage inverter of I² logic; 55

Figure 2 is an equivalent circuit diagram of a two-stage inverter of static induction transistor logic;

Figure 3 is a schematic sectional view of static induction transistor logic; 60

Figure 4 is a schematic sectional view of conventional I² logic;

Figure 5 illustrates the operation of the inverter of Figure 1; 65

Figure 6 is a schematic sectional view of one embodiment of a static induction transistor according to the present invention; and

Figure 7 illustrates one method of making a static induction transistor according to the present invention. 70

In the drawings, like parts have been designated by the same reference numerals. 75

Figures 1 and 2 respectively show equivalent circuits of two-stage inverters using I² logic and static induction transistor logic. Both circuits have an injector PNP transistor 1 but in the case of static induction transistor logic an N-channel static induction transistor 3 is used instead of a vertical NPN transistor 2 used in the I² logic. 80

Figure 3 shows in section a semi-conductor device for use in the static induction transistor logic of Figure 2 and Figure 4 shows in section a semi-conductor device for use in the I² logic of Figure 1. 85

In Figure 3, a substrate 4 of N⁺ conductivity type material has an epitaxial layer 5 of N⁻ conductivity type material grown thereon. The base of the transistor 1 is constituted by the substrate 4 and the layer 5 and the substrate 4 also forms the source of the transistor 3. P⁺ conductivity 90 95

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type diffusion regions 6, 8 are formed in the layer 5, the region 6 acting as the collector of the transistor 1 and the gate of the transistor 3. The region 8 acts as the emitter of the transistor 1. A diffusion region 7 of N^+ conductivity type material acts as the drain of the transistor 3. An oxide film 9 is formed on the layer 5.

In Figure 4, a substrate 10 of N^+ conductivity type material has an epitaxial layer 11 of N^- conductivity type material grown thereon. The base of the transistor 1 and the emitter of the transistor 2 are constituted by the substrate 10 and the layer 11. Diffusion regions 12, 14 of P^+ conductivity type material are formed in the layer 11, the region 12 acting as the collector of the transistor 1 and the base of the transistor 2. The region 14 acts as the emitter of the transistor 1. A diffusion region 13 of N^+ conductivity type material acts as the collector of the transistor 2. An oxide film 15 is formed on the layer 11.

The operation of the static induction transistor logic of Figure 2 will be described with reference to Figure 5. Since the impurity concentration of the epitaxial layer 5 is relatively very low, normally about 10^{13}cm^{-3} , a channel region 16 of the transistor 3 has already been pinched off when the gate voltage is zero. The channel region 16 is surrounded by the region 6 acting as the gate of the transistor 3. The characteristics of a voltage V_{DS} between the drain and the source of the transistor 3 and the current I_{DS} flowing between the drain and the source is an exponential function illustrated by curve 17. This is the so-called static induction transistor mode. When a gate voltage (generally about 0.7 V) is applied to make the pn junction between the gate and the source conductive, electrons are injected from the source into the channel region and the V_{DS} - I_{DS} characteristics rise sharply as illustrated by curve 18. This is the so-called charge injection mode. Curve 19 illustrates the load-line of the transistor 1 and, when the input voltage of the gate of the transistor 1 is zero, the action point is at 20 and the output voltage V_{DS} becomes "1". Inversely, when the input voltage is "1", the action point is at 21 and the output voltage V_{DS} becomes zero. As described above, the operation of static induction transistor logic is similar to that of I^2 logic. However, the static induction transistor logic has the very great advantage that its delay time is smaller by an order of magnitude and the delay time of I^2 logic because its junction capacitance is also smaller by an order of magnitude since the impurity concentration of the epitaxial layer 5 is smaller by two orders of magnitude compared to that of I^2 logic. However, when the gate voltage is zero, the current I_{DS}

shows exponential characteristics illustrated by curve 17 so that an unexpected large current—the so-called "off current"—can flow as a result of fluctuations across-the-channel due to the impurity concentrations in the P^+ conductivity type diffusion regions and the channel region.

The present invention thus seeks to provide static induction transistor logic having a lower power consumption than conventional static induction transistor logic by eliminating the above-mentioned disadvantage.

Figure 6 illustrates one embodiment of a static induction transistor according to the present invention. The static induction transistor logic of Figure 1 bears considerable similarity to the static induction transistor logic of Figure 2 except for the addition of region 22 of P^+ conductivity type material. The region 22 exists in the channel region of the transistor 3 and acts as a potential barrier to electrons flowing from the substrate 4 to the region 7 thus reducing the current I_{DS} . Whilst the subsequent reduction in the "off current" is also accompanied by a corresponding decrease in the "on current" i.e. the current flowing when the gate voltage exceeds a given level, the static induction transistor logic is such that the sharp rise of the current I_{DS} , indicated in Figure 5 by curve 18, still exists if the recombination of electrons with holes is prevented by reducing the impurity concentration of the region 22 and reducing the thickness of the region 22.

One method of making a static induction transistor according to the present invention will now be described with reference to Figure 7. Initially part of the epitaxial layer 5 is grown on the substrate 4 (Figure 7 (A)). Secondly, impurities 22 are thinly deposited in the channel region (Figure 7 (B)). Next the remainder of the layer 5 is grown (Figure 7 (C)). Thereafter the regions of P^+ conductivity type material for the gates of transistor 3 and the region 8 of the emitter are formed by a diffusion technique (Figure 7 (D)). The regions 6, 8 may be formed by an ion implantation technique to prevent expansion of the regions 22 as a result of diffusion of the regions 6, 8. Next, the regions 7 are thinly diffused into the layer 5 (Figure 7 (E)). Thereafter, the oxide film 9 with apertures for electrodes 23 is formed (Figure 7 (F)). Finally, the electrodes 23 are evaporated thereon to perform the wiring of the static induction transistor (Figure 7 (G)).

WHAT WE CLAIM IS:—

1. A static induction transistor having a drain region; a source region; a gate region; a channel surrounded by the gate region, and an impurity region of the same



type diffusion regions 6, 8 are formed in the layer 5, the region 6 acting as the collector of the transistor 1 and the gate of the transistor 3. The region 8 acts as the emitter of the transistor 1. A diffusion region 7 of N^+ conductivity type material acts as the drain of the transistor 3. An oxide film 9 is formed on the layer 5.

In Figure 4, a substrate 10 of N^+ conductivity type material has an epitaxial layer 11 of N^- conductivity type material grown thereon. The base of the transistor 1 and the emitter of the transistor 2 are constituted by the substrate 10 and the layer 11. Diffusion regions 12, 14 of P^+ conductivity type material are formed in the layer 11, the region 12 acting as the collector of the transistor 1 and the base of the transistor 2. The region 14 acts as the emitter of the transistor 1. A diffusion region 13 of N^+ conductivity type material acts as the collector of the transistor 2. An oxide film 15 is formed on the layer 11.

The operation of the static induction transistor logic of Figure 2 will be described with reference to Figure 5. Since the impurity concentration of the epitaxial layer 5 is relatively very low, normally about 10^{13}cm^{-3} , a channel region 16 of the transistor 3 has already been pinched off when the gate voltage is zero. The channel region 16 is surrounded by the region 6 acting as the gate of the transistor 3. The characteristics of a voltage V_{DS} between the drain and the source of the transistor 3 and the current I_{DS} flowing between the drain and the source is an exponential function illustrated by curve 17. This is the so-called static induction transistor mode. When a gate voltage (generally about 0.7 V) is applied to make the pn junction between the gate and the source conductive, electrons are injected from the source into the channel region and the $V_{DS}-I_{DS}$ characteristics rise sharply as illustrated by curve 18. This is the so-called charge injection mode. Curve 19 illustrates the load-line of the transistor 1 and, when the input voltage of the gate of the transistor 1 is zero, the action point is at 20 and the output voltage V_{DS} becomes "1". Inversely, when the input voltage is "1", the action point is at 21 and the output voltage V_{DS} becomes zero. As described above, the operation of static induction transistor logic is similar to that of I^2 logic. However, the static induction transistor logic has the very great advantage that its delay time is smaller by an order of magnitude and the delay time of I^2 logic because its junction capacitance is also smaller by an order of magnitude since the impurity concentration of the epitaxial layer 5 is smaller by two orders of magnitude compared to that of I^2 logic. However, when the gate voltage is zero, the current I_{DS}

shows exponential characteristics illustrated by curve 17 so that an unexpected large current—the so-called "off current"—can flow as a result of fluctuations across-the-channel due to the impurity concentrations in the P^+ conductivity type diffusion regions and the channel region.

The present invention thus seeks to provide static induction transistor logic having a lower power consumption than conventional static induction transistor logic by eliminating the above-mentioned disadvantage.

Figure 6 illustrates one embodiment of a static induction transistor according to the present invention. The static induction transistor logic of Figure 1 bears considerable similarity to the static induction transistor logic of Figure 2 except for the addition of region 22 of P^+ conductivity type material. The region 22 exists in the channel region of the transistor 3 and acts as a potential barrier to electrons flowing from the substrate 4 to the region 7 thus reducing the current I_{DS} . Whilst the subsequent reduction in the "off current" is also accompanied by a corresponding decrease in the "on current" i.e. the current flowing when the gate voltage exceeds a given level, the static induction transistor logic is such that the sharp rise of the current I_{DS} , indicated in Figure 5 by curve 18, still exists if the recombination of electrons with holes is prevented by reducing the impurity concentration of the region 22 and reducing the thickness of the region 22.

One method of making a static induction transistor according to the present invention will now be described with reference to Figure 7. Initially part of the epitaxial layer 5 is grown on the substrate 4 (Figure 7 (A)). Secondly, impurities 22 are thinly deposited in the channel region (Figure 7 (B)). Next the remainder of the layer 5 is grown (Figure 7 (C)). Thereafter the regions of P^+ conductivity type material for the gates of transistor 3 and the region 8 of the emitter are formed by a diffusion technique (Figure 7 (D)). The regions 6, 8 may be formed by an ion implantation technique to prevent expansion of the regions 22 as a result of diffusion of the regions 6, 8. Next, the regions 7 are thinly diffused into the layer 5 (Figure 7 (E)). Thereafter, the oxide film 9 with apertures for electrodes 23 is formed (Figure 7 (F)). Finally, the electrodes 23 are evaporated thereon to perform the wiring of the static induction transistor (Figure 7 (G)).

WHAT WE CLAIM IS:—

1. A static induction transistor having a drain region; a source region; a gate region; a channel surrounded by the gate region, and an impurity region of the same



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conductivity type as the gate region the impurity region extending completely across the channel region and being disposed between and spaced from the drain region and the source region.

2. A static induction transistor as claimed in claim 1 in which the gate region and the said impurity region are of P³ conductivity type material.

3. A static induction transistor as claimed in claim 1 or 2 in which the drain region is surrounded by the gate region.

4. A static induction transistor substantially as hereindescribed with reference to and shown in Figure 6 of the accompanying drawings.

5. An inverter including a static induction transistor as claimed in any preceding claim.

6. A method of making a static induction transistor having a drain region; a source region; a gate region; and a channel region surrounded by the gate region including forming an impurity region of the same conductivity type as the gate region the

impurity region extending completely across the channel region and being disposed between and spaced from the drain region and the source region.

7. A method as claimed in claim 6 in which the first part of an epitaxial layer is grown on a substrate, the said impurity region is formed in said first part of the epitaxial layer, and the second part of the epitaxial layer is then grown and the gate region and the drain region are then formed in the second part of the epitaxial layer.

8. A method of making a static induction transistor substantially as herein described with reference to Figure 7 of the accompanying drawings.

J. MILLER & CO.,
Chartered Patent Agents,
Agents for the Applicants,
Lincoln House,
296—302 High Holborn,
London, WC1V 7JH.