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METHOD OF FABRICATING A SILICON MICROPHONE

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FIELD OF THE INVENTION

The invention relates generally to the fabrication of condenser microphones and, more particularly, to methods of fabricating a CMOS device integrated with a condenser microphone that is formed on a CMOS n-well, a stand-alone condenser microphone formed on an n-well, and a stand-alone condenser microphone formed on an n-type epitaxial layer.

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BACKGROUND OF THE INVENTION

A condenser microphone (henceforth "the sensor") is a capacitive transducer that converts acoustic energy to electrical energy. The sensor typically comprises two parallel plates of any shape separated by an air gap. One of the plates ("the diaphragm") is such that it vibrates when sound energy impinges on it, while the other plate ("the backplate") is built in such a way that it remains rigid. The backplate includes at least one slot which allows air to flow into and out of the air gap.

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The vibration of the diaphragm, with respect to the backplate, generates a change in the capacitance of the sensor. If a bias charge "Q" is present on the sensor when the plates are in steady state, then according to the equation $Q = CV$, the change in the capacitance results in a proportional change in the voltage across the capacitor which conserves the charge.

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The condenser microphone has been well established for sound detection since the beginning of this century. Recently, solid state condenser microphones have been fabricated using well-established semiconductor techniques. Currently considerable research is being carried out to fabricate a silicon microphone along with an amplifier and bias circuit on the same chip. For this reason the fabrication process used for a condenser microphone should be such that they integrate smoothly with the commercial CMOS processes.

One technique in the fabrication of conventional silicon microphones uses heavily doped boron junctions (as the etch stop) to create a silicon diaphragm with a plated metal backplate. However, this technique is not CMOS compatible since the heavily doped boron junctions typically require a depth of about $3\text{ }\mu\text{m}$ for diaphragm fabrication which is generally not included in CMOS fabrication processes. Another conventional technique utilizes a low pressure chemical vapor deposition (LPCVD) nitride diaphragm (e.g., 0.25 to $1\text{ }\mu\text{m}$ thick). However, since the LPCVD nitride is deposited at temperatures of approximately 800°C , the formation of the diaphragm can not be performed after metallization, thereby disrupting the normal CMOS fabrication process. In a further technique, a silicon diaphragm and a silicon backplate are fabricated separately and thereafter bonded together using wafer to wafer bonding techniques. This, however, causes potentially large parasitic capacitance.

17 MAY 2002

It is therefore an object of the present invention to provide a process of fabricating a condenser microphone that is integrated into a CMOS device such that the microphone is formed at the end of the CMOS process using a CMOS n-well as the diaphragm.

5 Another object of the invention is to provide a stand-alone condenser microphone formed on an n-well of a silicon substrate, where the n-well forms the basis of the diaphragm.

 A further object of the invention is to provide a stand-alone condenser microphone formed on an n-epitaxial layer on a silicon substrate, where the
10 n-epitaxial layer forms the basis of the diaphragm.

Various other objects, advantages and features of the present invention will become readily apparent from the ensuing detailed description and the novel features which will be particularly pointed out in the appended claims.

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SUMMARY OF THE INVENTION

These and other objectives are realized the present invention. In a first fabrication process in accordance with the invention, a complementary metal oxide semiconductor (CMOS) and a sensor, having a backplate and a
20 diaphragm, are integrated on a single silicon p-substrate. Briefly, the sensor fabrication process begins after the completion of the CMOS fabrication process. Such process occurs without changes to the characteristics of the already fabricated CMOS circuitry. The prior fabrication of the CMOS circuitry includes diffusing impurities, such as phosphorus, into selected

regions of the substrate using known CMOS fabrication procedures to form a plurality of CMOS well regions. A selected one of the well regions will form the sensor region where the sensor will be subsequently fabricated.

Preferably, the sensor region is subsequently covered by an ILD (inter layer

5 dielectric) oxide layer followed by contact hole formation. The contact hole

formation includes metallization, patterning and etching steps to form a

metal contact pad with the epitaxial layer. The sensor region is then covered

by a PECVD (plasma enhance chemical vapor deposition) nitride as the

passivation layer. The sensor may now be fabricated using the following

10 preferred process:

1. etching portions of the first nitride and first oxide layers over the sensor region to expose the well region, wherein the exposed well region is the sensor diaphragm (this etching step may be performed during the etching step to expose the metal pad during the CMOS fabrication);

15 2. depositing a second oxide layer on the first nitride layer and exposed well region;

3. forming a plurality of trenches into the second oxide layer and the well region to form silicon springs;

4. removing the second oxide layer;

20 5. depositing a third oxide layer on the first nitride layer, exposed well region and silicon springs, wherein the third oxide layer is a sacrificial layer;

6. depositing a second nitride layer (preferably 3 μm thick) on the sacrificial layer, wherein the second nitride layer is the sensor backplate;

7. etching portions of said the backplate and sacrificial layer to form acoustic holes; and

8. removing the remaining portions of the sacrificial layer, except for the portions of the sacrificial layer immediately surrounding the sensor region, to form an air-gap cavity between the backplate and diaphragm.

Preferably, a metallic layer, such as aluminum is deposited on the backplate, such that the step of etching further includes etching portions of the aluminum layer. Illustratively, the sacrificial layer is planarized using a spin-on-glass (SOG) technique. The step of removing the sacrificial layer is preferably performed by a step of wet etching. Further, the reverse side of the substrate may be electrochemically etched (ECE) using the well region as an etch stop, where KOH is the ECE etchant. The reverse side is etched in a flat v-shape area, such that the thickness of the diaphragm is preferably 3 μm thick.

15 In a second fabrication process in accordance with the invention, a sensor is integrated on a silicon p-substrate, where the sensor has a backplate and a diaphragm. The sensor may now be fabricated using the following preferred process:

1. depositing a first oxide layer on the substrate;
- 20 2. etching a portion of the first oxide layer to expose the substrate;
3. implanting n-type material, preferably phosphorus, into the exposed substrate to form an n-well region, wherein the well region is the sensor diaphragm;

4. forming a plurality of trenches into the well region to form silicon springs;

5. depositing a second oxide layer over the well region and the silicon springs, wherein the second oxide layer is the sacrificial layer;

5 6. depositing a nitride layer on the sacrificial layer, wherein the nitride layer is the sensor backplate;

7. etching portions of the backplate and the sacrificial layer to form acoustic holes; and

8. removing the sacrificial layer to form a cavity between the
10 backplate and the diaphragm.

Preferably, the above process also includes the steps of implanting arsenic into the well region to form source and drain regions, and annealing the source and drain regions to improve its contact resistance to metal.

In a third fabrication process in accordance with the invention, a
15 sensor is integrated on an n-type epitaxial layer formed on a silicon p-substrate, where the sensor has a backplate and a diaphragm. The sensor may now be fabricated using the following preferred process:

1. depositing a first oxide layer on the epitaxial layer;

2. etching a portion of the first oxide layer to expose the epitaxial
20 layer, wherein the exposed epitaxial layer is the sensor diaphragm;

3. forming a plurality of trenches into the epitaxial layer to form silicon springs;

4. depositing a second oxide layer over the epitaxial layer and the silicon springs, wherein the second oxide layer is the sacrificial layer;

5. depositing a nitride layer on the sacrificial layer, wherein the nitride layer is the sensor backplate;

6. etching portions of the backplate and the sacrificial layer to form acoustic holes; and

5 7. removing the sacrificial layer to form a cavity between the backplate and the diaphragm.

Similarly, the above process preferably includes the steps of implanting arsenic into the epitaxial layer to form source and drain regions, and annealing the source and drain regions to improve its contact resistance
10 to metal.

BRIEF DESCRIPTION OF THE DRAWINGS

The following detailed description, giving by way of example and not intended to limit the present invention solely thereto, will best be understood
15 in conjunction with the accompanying drawings in which:

FIGs 1A-1K show the fabrication steps in forming a sensor that is integrated into a CMOS device in accordance with a first process of the present invention.

FIGs 2 illustrates the change of sensor sensitivity over frequency for
20 air gaps of various thicknesses.

FIGs 3A-3E show the fabrication steps in forming a stand-alone sensor formed on an n-well of a silicon substrate in accordance with a second process of the present invention.

FIGs 4A-4D show the fabrication steps in forming a stand-alone sensor formed on an n-type epitaxial layer on a silicon substrate in accordance with a third process of the present invention.

5 **DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS**

FIGs 1A - 1K show a first fabrication process in accordance with the present invention. Specifically, FIGs 1A-1K show a process for fabricating a sensor that is integrated with a CMOS device 5 on a silicon substrate 10. Although a p-type silicon substrate is illustrated, it will be understood that
10 other substrates having opposite conductivities may be used as well. The formation of the sensor begins at the end of a typical CMOS fabrication process. Note, however, that the fabrication of the sensor does not alter any of the characteristics of the CMOS device 5 shown in Fig 1A.

FIG 1A shows a CMOS device 5 that is divided into three sections, A,
15 B and C. Illustratively, section B is a p-MOS device and section C is an n-MOS device formed on the same p-type substrate 10 (section A is the section in which the sensor will be subsequently fabricated). With respect to section B, the p-MOS device includes p+ source and drain regions 18 separated by a gate 19. Source and drain regions 18 are formed in an n-well
20 16. Similarly, the n-MOS device of section C includes n+ source and drain regions 22 separated by a gate 21. In the n-MOS device, source and drain regions 22 are formed in a p-well 20.

CMOS device 5 also includes an area in which the sensor will be formed, i.e., section A, having an n-well 12. For example, the n-well may be formed by the implantation of phosphorous. Illustratively, a metal contact pad 14, which is preferably formed of aluminum, is formed to connect the active regions 8 of n-well 12 to the surface. The n-well is made active by implanting n+ arsenic (As) to form the source and drain 8. The active region is then annealed to improve its contact resistance to metal.

Overlaying the sections A, B, and C are a BPSG/field oxide layer 24 and a plasma enhance chemical vapor deposition (PECVD) passivation nitride layer 26. BPSG/field oxide layer 24 includes a borophosphorus silicate glass (BPSG) layer 27 formed on the n-wells and a field oxide layer 28 formed on the BPSG layer.

FIGs 1B - 1J illustrate the process of fabricating the sensor (in section A) of CMOS device 5. FIG 1B shows a sensor area 30 which has been opened by etching a portion of the nitride layer 26 and BPSG/field oxide layer 24. The next step includes depositing a PECVD masking oxide layer 34 on the top surface of nitride layer 26 and n-well 12. A photo resist mask 36 is then deposited on oxide layer 34 to form slots 32. The slots are patterned in photoresist on oxide layer 34 and the oxide layer is dry etched. This is illustrated in FIG 1C. Thereafter, the photoresist is removed, using oxide layer 34 as a mask, and the slots 32 and oxide layer 34 are etched, by silicon reactive ionization etching (RIE), to form silicon springs 40. Illustratively, the trenches are 3 μm in depth. Photo resist mask 36 and

oxide 34 are then removed using a global dry etch. The result is illustrated in FIG 1D.

FIG 1E shows a PECVD oxide layer 42, i.e., the sacrificial layer, deposited on the top layer of the device of FIG 1D. Note that sacrificial oxide layer 42 is illustratively 3 μm thick. Using a standard spin-on-glass (SOG) planarization technique, the sacrificial layer is planarized to form planarized sacrificial layer 44, as shown in FIG 1F.

Next, a second PECVD nitride layer 46 is deposited on planarized sacrificial layer 44. Preferably, nitride layer 46 is 3 μm thick. Note that nitride layer 46 forms the backplate of the sensor. Further, a metallic layer 48 is deposited on nitride layer 46. Illustratively, metallic layer 48 is aluminum having a depth of 1 μm . The nitride and metallic layer 46, 48 are shown in FIG 1G.

In FIG 1H, photo resist mask layer 50 is shown deposited on metallic layer 48. Thereafter, the metallic and nitride layers 48, 46 are dry etched to form acoustic holes 52, and the metallic layer 48, nitride layer 46 and sacrificial oxide layer 44 are dry etched to expose areas 54 and 56.

At this point, a layer of TiN is deposited on the front (polished) side of the device of FIG 1I to connect all of the exposed n-wells (not shown).

Further, the reverse side of the device may optionally be electrochemically etched (ECE) through the silicon substrate 11 and n-well 12 using KOH as the etchant, to form a flat V-shape area 70 through p-substrate 10 and n-well 12 (FIG 1K). Preferably, the thickness of the remaining silicon n-well above the etched area (i.e., the diaphragm) is 3 μm . Note that in the ECE

process, the n-well is used as an etch stop. In addition, it is noted that the reverse side of the substrate may also have a stress release oxide (SRO) grown on the p-type substrate which is followed by a LPCVD nitride layer. This nitride layer is used as an etching mask for the KOH etching. Further, a protective PECVD oxide is deposited on the LPCVD nitride layer.

Referring now to FIG 1J, the TiN layer is removed and sacrificial oxide layer 44 is wet etched which releases the microphone backplate and forms air gap 60. Note that small portions of the sacrificial oxide layer, between layers 26 & 46, optionally remain as oxide pads 62. FIG 1K shows the completed CMOS device having an integrated sensor therein.

FIG 2 illustrates the change of sensitivity (dB ref 1 V/pa) of the sensor over frequency (Hz). Note that this graph illustrates change in sensitivity for different thicknesses of air gap 60. Specifically, the air gap is shown having a thicknesses of 3, 4, 5 and 6 μm . Recall that the thickness of air gap 60 depends on the thickness of the sacrificial layer.

In a second fabrication process in accordance with the present invention, a stand-alone sensor is formed on an n-well in a silicon substrate. Specifically, a layer of PECVD oxide 124 is deposited on a p-substrate 110. Illustratively, oxide layer 124 is 1 μm thick. This is shown in FIG 3A. Oxide layer 124 is then masked (not shown) and etched to open a flat V-shape sensor area 130. Thereafter, a thin stress release oxide (SRO) layer 123 is optionally grown in sensor area 130. Sensor area 130 and SRO layer 123 are shown in FIG 3B.

FIG 3C shows an n- implantation of, e.g., phosphorous, into p-substrate 110, through sensor area 130. Preferably, the phosphorous implantation (which forms the n-well) is implanted 3 μm deep. FIG 3D shows arsenic (As) being implanted into n-well 112 to form source and drain regions 108. Afterwards, the As implanted region is annealed to improve the contact resistance to metal.

At this stage, the SRO layer is etched away and a metallic oxide pad 114 is deposited. Preferably, pad 114 is formed of aluminum. Thereafter, a layer of PECVD nitride 126 is deposited on the device. Nitride layer 126 is then masked and etched (not shown) to expose pad 114 and the active region of n-well 112.

The remaining steps in forming the above described sensor are substantially identical to the steps performed with reference to FIGs 1B - 1J. Accordingly, such steps will not be redescribed.

In a third fabrication process in accordance with the present invention, a stand-alone sensor is formed on an n-epitaxial layer on a silicon substrate. As shown in FIG 4A, an n-type epitaxial layer 213 is formed on the p-substrate 210. Illustratively, the epitaxial layer is 8 μm thick. Further, a PECVD oxide layer is formed on epitaxial layer 213. Oxide layer 224 is preferably 1 μm thick. Oxide layer 224 is then masked (not shown) and etched to open a flat V-shape sensor area 230. Thereafter, an SRO layer 223 is optionally grown in sensor area 230. Sensor area 230 and SRO layer 223 are shown in FIG 4B.

FIG 4C shows arsenic (As) being implanted into the epitaxial layer to form source and drain regions 208. Afterward, the arsenic implanted region is annealed. At this stage, the SRO layer is etched away and a metallic oxide pad 214 is deposited. Preferably, pad 214 is formed of aluminum.

- 5 Thereafter, a layer of PECVD nitride 226 is deposited on the device. Nitride layer 226 is then masked and etched (not shown) to expose pad 214 and the active region of epitaxial layer 213.

The remaining steps in forming the above described sensor are substantially identical to the steps formed with reference to FIGs 1B-1J.

- 10 Accordingly, such steps will not be re-described.

While several embodiments have been chosen to illustrate the invention, it will be understood by those skilled in the art that various changes and modifications can be made herein without departing from the scope or spirit of the invention as defined in the appended claims.

WHAT IS CLAIMED IS:

1. A method for fabricating a sensor that is integrated with a previously formed complementary metal oxide semiconductor (CMOS) on a
5 single silicon substrate having a first conductivity type, said sensor having a backplate and a diaphragm, wherein the prior fabrication of said CMOS circuitry includes diffusing impurities having a second conductivity type into selected regions of said substrate to form a plurality of CMOS well regions, wherein one of said well regions being a sensor region indicating where said
10 sensor will be subsequently fabricated, said method comprising the steps of:
 - a. etching said sensor region to expose said well region, wherein the exposed well region being said diaphragm;
 - b. forming a plurality of trenches into said well to form silicon
springs;
 - 15 c. depositing an oxide layer over said exposed well region and said silicon springs, said oxide layer being a sacrificial layer;
 - d. depositing a nitride layer on said sacrificial layer, said nitride layer being said backplate;
 - e. etching portions of said backplate and said sacrificial layer to
20 form acoustic holes; and
 - f. removing said sacrificial layer to form a cavity between said backplate and said diaphragm.

2. The method of claim 1 further comprising the step of:

d1. depositing a metallic layer on said backplate, wherein the step of etching further includes etching portions of said metallic layer.

3. The method of claim 2, wherein said metallic layer is aluminum.

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4. The method of claim 1, wherein said first conductivity type is p-type and said second conductivity type is n-type.

5. The method of claim 1, further comprising a step of etching the reverse side of said silicon substrate and said well region such that the thickness of said diaphragm is approximately 3 μm .

6. The method of claim 5, wherein said step of etching the reverse side is performed by a step of electrochemical etching (ECE) using said well region as an etch stop, wherein KOH is used as the etchant for performing said ECE.

7. The method of claim 1 further comprising the step of:

d1. planarizing said sacrificial layer using a spin-on-glass (SOG) technique.

8. The method of claim 1, wherein the thickness of said backplate is 3 μm .

9. A method for fabricating a sensor that is integrated with a previously formed complementary metal oxide semiconductor (CMOS) on a single silicon substrate having a first conductivity type, said sensor having a backplate and a diaphragm, wherein the prior fabrication of said CMOS

5 circuitry includes forming a first nitride layer on a first oxide layer, and diffusing impurities having a second conductivity type into selected regions of said substrate to form a plurality of CMOS well regions, wherein one of said well regions being a sensor region indicating where said sensor will be subsequently fabricated, said method comprising the steps of:

10 a. etching portions of said first nitride and first oxide layers over said sensor region to expose said well region, wherein the exposed well region being said diaphragm;

b. depositing a second oxide layer on said first nitride layer and exposed well region;

15 c. forming a plurality of trenches into said second oxide layer and said well region to form silicon springs;

d. removing said second oxide layer;

e. depositing a third oxide layer on said first nitride layer, exposed well region and silicon springs, said third oxide layer being a sacrificial layer;

20 f. depositing a second nitride layer on said sacrificial layer, said second nitride layer being said backplate;

g. etching portions of said backplate and said sacrificial layer to form acoustic holes; and

h. removing the remaining portions of said sacrificial layer, except for portions of said sacrificial layer immediately surrounding said sensor region, to form an air-gap cavity between said backplate and said diaphragm.

5 10. The method of claim 9 further comprising the step of:

 f1. depositing a metallic layer on said backplate, wherein the step of etching further includes etching portions of said metallic layer.

 11. The method of claim 10, wherein said metallic layer is
10 aluminum.

 12. The method of claim 9, wherein said first conductivity type is p-type and said second conductivity type is n-type.

15 13. The method of claim 9, further comprising a step of etching the reverse side of said silicon substrate and said well region such that the thickness of said diaphragm is approximately 3 μm .

14. The method of claim 13, wherein said step of etching the reverse side is performed by a step of electrochemical etching (ECE) using said well region as an etch stop, wherein KOH is used as the etchant for performing said ECE.

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15. The method of claim 9 further comprising the step of:

e1. planarizing said sacrificial layer using a spin-on-glass (SOG) technique.

10 16. The method of claim 9, wherein the thickness of said backplate is 3 μm .

17. A method for fabricating a sensor integrated on a silicon substrate having a first conductivity type, said sensor having a backplate and
15 a diaphragm, comprising the steps of:

- a. depositing a first oxide layer on said substrate;
- b. etching a portion of said first oxide layer to expose said substrate;
- c. implanting material of a second conductivity type into said
20 exposed substrate to form an n-well region, wherein the well region being said diaphragm;
- d. forming a plurality of trenches into said well region to form silicon springs;

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e. depositing a second oxide layer over said well region and said silicon springs, said second oxide layer being a sacrificial layer;

f. depositing a nitride layer on said sacrificial layer, said nitride layer being said backplate;

5 g. etching portions of said backplate and said sacrificial layer to form acoustic holes; and

h. removing said sacrificial layer to form a cavity between said backplate and said diaphragm.

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18. The method of claim 17 further comprising the steps of:

c1. implanting arsenic into said well region to form source and drain regions; and

c2. annealing said source and drain regions to improve the source
15 and drain regions contact resistance to metal.

19. The method of claim 18 further comprising the step of:

c3. depositing a metallic layer on said backplate, wherein the step of etching further includes etching portions of said metallic layer.

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20. The method of claim 19, wherein said metallic layer is aluminum.

21. The method of claim 17, wherein said first conductivity type is p-type and said second conductivity type is n-type.

22. The method of claim 21, wherein said step of implanting a
5 second conductivity type material is n- phosphorus.

23. The method of claim 17, further comprising a step of etching the reverse side of said silicon substrate and said well region such that the thickness of said diaphragm is approximately 3 μm .

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24. The method of claim 23, wherein said step of etching the reverse side is performed by a step of electrochemical etching (ECE) using said well region as an etch stop, wherein KOH is used as the etchant for performing said ECE.

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25. The method of claim 17 further comprising the step of:

e1. planarizing said sacrificial layer using a spin-on-glass (SOG) technique.

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26. The method of claim 17, wherein the thickness of said backplate is 3 μm .

27. A method for fabricating a sensor integrated on an epitaxial layer, having a second conductivity type, formed on a silicon substrate

having a first conductivity type, said sensor having a backplate and a diaphragm, comprising the steps of:

- a. depositing a first oxide layer on said epitaxial layer;
- b. etching a portion of said first oxide layer to expose said epitaxial layer, the exposed epitaxial layer being said diaphragm;
- c. forming a plurality of trenches into said epitaxial layer to form silicon springs;
- d. depositing a second oxide layer over said epitaxial layer and said silicon springs, said second oxide layer being a sacrificial layer;
- 10 e. depositing a nitride layer on said sacrificial layer, said nitride layer being said backplate;
- f. etching portions of said backplate and said sacrificial layer to form acoustic holes; and
- g. removing said sacrificial layer to form a cavity between said
- 15 backplate and said diaphragm.

28. The method of claim 27 further comprising the steps of:

- b1. implanting arsenic into said epitaxial layer to form source and drain regions; and
- b2. annealing said source and drain regions to improve the source
- 20 and drain regions contact resistance to metal.

29. The method of claim 28 further comprising the step of:

- b3. depositing a metallic layer on said backplate, wherein the step of etching further includes etching portions of said metallic layer.

30. The method of claim 29, wherein said metallic layer is aluminum.

31. The method of claim 27, wherein said first conductivity type is
5 p-type and said second conductivity type is n-type.

32. The method of claim 27, further comprising a step of etching
the reverse side of said silicon substrate and said well region such that the
thickness of said diaphragm is approximately 3 μm .

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33. The method of claim 32, wherein said step of etching the
reverse side is performed by a step of electrochemical etching (ECE) using
said well region as an etch stop, wherein KOH is used as the etchant for
performing said ECE.

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34. The method of claim 27 further comprising the step of:
- e1. planarizing said sacrificial layer using a spin-on-glass (SOG) technique.

- 5 35. The method of claim 27, wherein the thickness of said backplate is 3 μm .