What is claimed is:

1. A method for forming a transistor, comprising:
forming a fin from a crystalline substrate;
forming a first source/drain region in the substrate beneath the fin;
forming a surrounding gate insulator around the fin;
forming a surrounding gate around the fin and separated from the fin by the surrounding gate insulator; and
forming a second source/drain region in a top portion of the fin.

2. The method of claim 1, wherein the fin has a cross-sectional thickness in a first direction corresponding to a minimum feature length and a cross-sectional thickness in a second direction orthogonal to the first direction less than the minimum feature length.

3. The method of claim 1, wherein forming a fin from a crystalline substrate includes forming a fin from a crystalline silicon substrate.

4. The method of claim 1, wherein forming a fin from a crystalline substrate includes etching the crystalline substrate to form the fin.

5. The method of claim 1, wherein forming a first source/drain region in the substrate beneath the fin includes implanting a dopant in a trench adjacent to the substrate and diffusing the dopant underneath the fin.

6. The method of claim 5, wherein diffusing includes diffusing the dopant into a bottom portion of the fin.

7. The method of claim 1, wherein forming a surrounding gate insulator includes forming a silicon oxide.

8. The method of claim 1, wherein forming a surrounding gate includes forming a polysilicon gate.

9. The method of claim 1, further comprising recessing the surrounding gate such that the surrounding gate has a height less than a height of the fin.

10. The method of claim 1, further comprising forming a gate contact adjacent to and in contact with the surrounding gate.

11. The method of claim 1, further comprising forming at least one gate line adjacent to and in contact with the surrounding gate.

12. The method of claim 11, wherein forming at least one gate line adjacent to and in contact with the surrounding gate includes forming a first gate line adjacent to and in contact with a first side of the surrounding gate and a second gate line adjacent to and in contact with a second side of the surrounding gate, the first and second sides being positioned on opposing sides of the fin.

13. The method of claim 11, wherein the fin has a rectangular footprint with a short side and a long side, wherein forming at least one gate line adjacent to and in contact with the surrounding gate includes forming a gate line to contact the surrounding gate on the long side.

14. The method of claim 11, wherein the fin has a rectangular footprint with a short side and a long side, wherein forming at least one gate line adjacent to and in contact with the surrounding gate includes forming a gate line to contact the surrounding gate on the short side.

15. The method of claim 1, wherein forming a surrounding gate includes forming a polysilicon surrounding gate.

16. A method for forming a transistor, comprising:

etching a fin from a crystalline silicon substrate, the fin having a cross-sectional thickness in a first direction corresponding to a minimum feature length and a cross-sectional thickness in a second direction orthogonal to the first direction less than the minimum feature length;

forming a first source/drain region in the substrate beneath the fin;

forming a surrounding gate oxide around the fin;

forming a polysilicon surrounding gate around the fin and separated from the fin by the surrounding gate oxide; and

forming a second source/drain region in a top portion of the fin.

17. The method of claim 16, wherein forming a surrounding gate oxide includes thermally oxidizing the silicon fin etched from the crystalline silicon substrate.

18. The method of claim 16, wherein etching a fin from a crystalline silicon substrate includes:

etching a hole in a layer over the substrate;

forming sidewall spacers in the hole;

forming a fin pattern from the sidewall spacers; and

etching into the crystalline substrate to form the fin from the substrate using a mask corresponding to the fin pattern.

19. A method for forming a transistor, comprising:

etching a fin from a crystalline substrate, the fin having a cross-sectional thickness in a first direction corresponding to a minimum feature length and a

cross-sectional thickness in a second direction orthogonal to the first direction less than the minimum feature length, wherein etching a fin includes:

etching a hole in a layer over the substrate;

forming sidewall spacers in the hole;

forming a fin pattern from the sidewall spacers;

etching into the crystalline substrate to form the fin from the substrate using a mask corresponding to the fin pattern;

forming a first source/drain region in the substrate beneath the fin;

forming a surrounding gate insulator around the fin;

forming a surrounding gate around the fin and separated from the fin by the surrounding gate insulator; and

forming a second source/drain region in a top portion of the fin.

20. The method of claim 19, wherein forming a surrounding gate oxide includes thermally oxidizing the silicon fin etched from the crystalline silicon substrate.

21. The method of claim 19, wherein forming a surrounding gate includes etching the gate so that the top of the gate is below the top surface of the fin.

22. A method for forming an array of transistors, comprising:

forming a nitride layer on a silicon wafer;

forming an amorphous silicon layer on the nitride layer;

patterning and etching at least one hole in the amorphous silicon layer;

oxidizing the amorphous silicon layer, which results in oxide sidewall spacers on sidewalls of the amorphous silicon layer;

backfilling the hole with amorphous silicon;

planarizing to expose the oxide sidewalls;

patterning and etching the oxide sidewalls into a fin pattern;

removing the amorphous silicon;

etching the nitride layer, leaving a fin pattern of nitride beneath the fin pattern of oxide sidewalls;

etching the silicon wafer, using the fin pattern of nitride as a mask, to etch silicon fins from the silicon wafer;

implanting dopant and diffusing the dopant to form a conduction line beneath the etched silicon fins, the dopant providing first source/drain regions for the silicon fins;

forming a surrounding gate insulator on the silicon fins;

forming a surrounding gate around and separated from the silicon fins by the surrounding gate insulator;

forming gate lines adjacent to and in contact with the surrounding gates for adjacent transistors in the array; and

forming second source/drain regions for the silicon fins.

23. The method of claim 22, wherein forming a surrounding gate insulator includes thermally oxidizing the silicon fin etched from the crystalline silicon substrate.

24. The method of claim 22, wherein forming a surrounding gate includes forming a polysilicon gate.

25. A transistor, comprising:

a crystalline substrate, with trenches etched therein to form a crystalline semiconductor fin from the substrate, the fin having a cross-sectional dimension that is less than a minimum feature size;

a first source/drain region formed in the crystalline substrate at a bottom of the fin, and a second source/drain region formed in a top portion of the fin to define a vertically-oriented channel region in the fin between the first and second source/drain regions;

a gate insulator formed around the fin; and

a surrounding gate formed around and separated from the fin by the gate insulator.

26. The transistor of claim 25, wherein the crystalline substrate includes silicon.

27. The transistor of claim 25, wherein the crystalline substrate is a crystalline silicon wafer.

28. The transistor of claim 25, wherein the surrounding gate insulator includes silicon oxide.

29. The transistor of claim 25, wherein the surrounding gate includes polysilicon.

30. The transistor of claim 25, wherein the surrounding gate includes metal.

31. A transistor, comprising:

a crystalline silicon wafer, with trenches etched therein to form a crystalline semiconductor fin from the wafer, the fin having a cross-sectional dimension in a first direction that is less than a minimum feature size and a cross-sectional dimension in a second direction orthogonal to the first direction that corresponds to the minimum feature size;

a first source/drain region formed in the crystalline wafer at a bottom of the fin, and a second source/drain region formed in a top portion of the fin to define a vertically-oriented channel region in the fin between the first and second source/drain regions;

a gate insulator formed around the fin; and

a surrounding gate formed around and separated from the fin by the gate insulator.

32. The transistor of claim 31, wherein the gate insulator includes a silicon oxide.

33. The transistor of claim 32, wherein the silicon oxide gate insulator is thermally-grown silicon oxide.

34. The transistor of claim 31, wherein the surrounding gate includes a polysilicon surrounding gate.

35. The transistor of claim 31, wherein the surrounding gate includes a metal surrounding gate.

36. A semiconductor structure, comprising:

an array of transistors arranged in columns and rows, each transistor including a first source/drain region, a second source/drain region above the first source/drain region, and a vertically-oriented channel region between the first and second source/drain regions, the channel region being formed in a crystalline semiconductor fin having a cross-sectional thickness that is less than a minimum feature size, the fin being formed from a crystalline wafer by etching trenches to define the fin, each transistor further including a gate insulator formed around the fin and a surrounding gate formed around and separated from the fin by the gate insulator.

37. The structure of claim 36, further comprising at least one gate line along the fins in contact with the surrounding gate.

38. The structure of claim 37, wherein the fin has a rectangular cross-section with a long side and a short side, and the at least one gate line contacts the surrounding gate on the short side.

39. The structure of claim 37, wherein the fin has a rectangular cross-section with a long side and a short side, and the at least one gate line contacts the surrounding gate on the short side.

40. The structure of claim 37, wherein the at least one gate line includes two gate lines on opposing sides of the fins.

41. The structure of claim 36, wherein a first row and an adjacent second row has a center-to-center spacing of a minimum feature size interval (NF) less the thickness of the fin structures, and the second row and an adjacent third row has a center-to-center spacing of the minimum feature size interval (NF) plus the thickness of the fin structures.

What is claimed is:

1. A method for forming a transistor, comprising:

forming a fin from a crystalline substrate, wherein forming the fin includes:

depositing a material on the crystalline substrate;

forming a mask pattern and using the mask pattern with a minimum feature length to etch the material to define at least two holes in the material, wherein the material provides sidewalls that surround and define each of the at least two holes, and wherein each of the at least two holes is one minimum feature length (F) wide and the at least two holes are separated by one minimum feature length (F);

forming sidewall spacers on each of the sidewalls that surround and define the at least two holes;

forming a fin pattern from the sidewall spacers, wherein forming the fin pattern includes forming an array of sidewall spacers, wherein a first row of the array and an adjacent second row of the array has a center-to-center spacing of the minimum feature length (F) less a thickness of the fin (ΔT), and the second row and an adjacent third row of the array has a center-to-center spacing of the minimum feature length (F) plus the thickness of the fin (ΔT); and

using the fin pattern as a mask to etch the fin from the crystalline substrate,

wherein the fin has a cross-sectional thickness in a first direction corresponding to the minimum feature length and a cross-sectional thickness in a second direction orthogonal to the first direction less than the minimum feature length,

wherein the first direction is substantially parallel to a surface of the substrate and the second direction is substantially parallel to the surface of the substrate;

forming a first source/drain region in the substrate beneath the fin;

forming a surrounding gate insulator around the fin;

forming a surrounding gate around the fin and separated from the fin by the surrounding gate insulator; and

forming a second source/drain region in a top portion of the fin.

2. The method of claim 1, wherein forming the fin from the crystalline substrate includes forming the fin from a crystalline silicon substrate.

3. The method of claim 1, wherein forming the first source/drain region in the substrate

beneath the fin includes implanting a dopant in a trench adjacent to the substrate and diffusing the dopant underneath the fin.

4. The method of claim 3, wherein diffusing includes diffusing the dopant into a bottom portion of the fin.

5. The method of claim 1, wherein forming the surrounding gate insulator includes forming a silicon oxide.

6. The method of claim 1, wherein forming the surrounding gate includes forming a polysilicon gate.

7. The method of claim 1, further comprising recessing the surrounding gate such that the surrounding gate has a height less than a height of the fin.

8. The method of claim 1, further comprising forming a gate contact adjacent to and in contact with the surrounding gate.

9. The method of claim 1, further comprising forming at least one gate line adjacent to and in contact with the surrounding gate.

10. The method of claim 9, wherein forming the at least one gate line adjacent to and in contact with the surrounding gate includes forming a first gate line adjacent to and in contact with a first side of the surrounding gate and a second gate line adjacent to and in contact with a second side of the surrounding gate, the first and second sides being positioned on opposing sides of the fin.

11. The method of claim 9, wherein the fin has a rectangular footprint with a short side and a long side, wherein forming the at least one gate line adjacent to and in contact with the surrounding gate includes forming a gate line to contact the surrounding gate on the long side.

12. The method of claim 9, wherein the fin has a rectangular footprint with a short side and a long side, wherein forming at least one gate line adjacent to and in contact with the

surrounding gate includes forming a gate line to contact the surrounding gate on the short side.

13. The method of claim 1, wherein forming the surrounding gate includes forming a polysilicon surrounding gate.

14. A method for forming a transistor, comprising:

etching a fin from a crystalline silicon substrate, wherein etching the fin from the crystalline substrate includes:

depositing a material on the crystalline substrate;

forming a mask pattern and using the mask pattern with a minimum feature length to etch the material to define at least two holes in the material, wherein the material provides sidewalls that surround and define each of the at least two holes, and wherein each of the at least two holes is one minimum feature length (F) wide and the at least two holes are separated by one minimum feature length (F); and

forming sidewall spacers on each of the sidewalls that surround and define the at least two holes;

forming a fin pattern from the sidewall spacers, wherein forming the fin pattern includes forming an array of sidewall spacers, wherein a first row of the array and an adjacent second row of the array has a center-to-center spacing of the minimum feature length (F) less a thickness of the fin (ΔT), and the second row and an adjacent third row of the array has a center-to-center spacing of the minimum feature length (F) plus the thickness of the fin (ΔT);

using the fin pattern as a mask to etch the fin,

wherein the fin has a cross-sectional thickness in a first direction corresponding to the minimum feature length and a cross-sectional thickness in a second direction orthogonal to the first direction less than the minimum feature length, and

wherein the first direction is substantially parallel to a surface of the substrate and the second direction is substantially parallel to the surface of the substrate;

forming a first source/drain region in the substrate beneath the fin;

forming a surrounding gate oxide around the fin;

forming a polysilicon surrounding gate around the fin and separated from the fin by the surrounding gate oxide; and

forming a second source/drain region in a top portion of the fin.

15. The method of claim 14, wherein forming the surrounding gate oxide includes thermally oxidizing the silicon fin etched from the crystalline silicon substrate.

16. The method of claim 14, wherein etching the fin from the crystalline silicon substrate includes:

etching a hole in a layer over the substrate;

forming sidewall spacers in the hole;

forming a fin pattern from the sidewall spacers; and

etching into the crystalline substrate to form the fin from the substrate using a mask corresponding to the fin pattern.

17. A method for forming an array of transistors, comprising:

forming a nitride layer on a silicon wafer;

forming an amorphous silicon layer on the nitride layer;

patterning and etching at least two holes in the amorphous silicon layer, wherein patterning includes using a mask pattern with a minimum feature length to pattern the at least two holes and etching includes using the mask pattern to etch the at least two holes, wherein the amorphous silicon layer provides sidewalls that surround and define each of the at least two holes, and wherein each of the at least two holes is one minimum feature length (F) wide and the at least two holes are separated by one minimum feature length (F);

oxidizing the amorphous silicon layer, which results in oxide sidewall spacers on each of the sidewalls of the amorphous silicon layer that surround and define the at least two holes;

backfilling the at least two holes with amorphous silicon;

planarizing to expose oxide sidewalls;

patterning and etching the oxide sidewalls into a fin pattern, wherein the fin pattern provides an array of sidewall spacers, wherein a first row of the array and an adjacent second row of the array has a center-to-center spacing of the minimum feature length (F) less a thickness of the fin (ΔT), and the second row and an adjacent third row of the array has a center-to-center spacing of the minimum feature length (F) plus a thickness of the fin (ΔT);

removing the amorphous silicon;

etching the nitride layer, leaving a fin pattern of nitride beneath the fin pattern of oxide sidewalls;

etching the silicon wafer, using the fin pattern of nitride as a mask, to etch silicon fins from the silicon wafer, wherein each of the silicon fins has a cross-sectional thickness in a

first direction corresponding to the minimum feature length and a cross-sectional thickness in a second direction orthogonal to the first direction less than the minimum feature length, wherein the first direction is substantially parallel to a surface of the silicon wafer and the second direction is substantially parallel to the surface of the silicon wafer;

implanting dopant and diffusing the dopant to form a conduction line beneath the etched silicon fins, the dopant providing first source/drain regions for the silicon fins;

forming a surrounding gate insulator on the silicon fins;

forming surrounding gates, wherein each surrounding gate is formed around and separated from one of the silicon fins by the surrounding gate insulator;

forming gate lines adjacent to and in contact with the surrounding gates for adjacent transistors in the array; and

forming second source/drain regions for the silicon fins.

18. The method of claim 17, wherein forming the surrounding gate insulator includes thermally oxidizing the silicon fin etched from the crystalline silicon substrate.

19. The method of claim 17, wherein forming the surrounding gates includes forming polysilicon gates.