

REGENERATIVE TIE-HIGH TIE-LOW CELL

ABSTRACT

5 A regenerative tie-high, tie-low cell (circuit) that
provides unconditionally stable logic (1 and 0) output
states used to tie off logic inputs. The circuit of this
invention eliminates any current flow through
p-channel/n-channel transistor pairs found in many
10 conventional circuits and adds a regenerative transistor
42 to assure rapid response in achieving the proper logic
output states. In one preferred embodiment, the circuit
consists of only three CMOS transistors 40-42 that reduce
the silicon area required, lowers the cost, and improves
15 the overall reliability.

Figure 4