METHOD OF SELF - ALIGNING A DAMASCENE GATE

STRUCTURE TO ISOLATION REGIONS

ABSTRACT

A process for fabricating a CMOS device in which conductive gate structures are defined self-aligned to shallow trench isolation (STI), regions, without using a photolithographic procedure, has been developed. The process features definition of shallow trench openings in regions of a semiconductor substrate not covered by dummy gate structures, or by silicon oxide spacers located on sides of the dummy gate structures. Filling of the shallow trench openings with silicon oxide, and removal of the dummy gate structures, result in STI regions comprised of filled shallow trench openings, overlying silicon oxide shapes, and silicon oxide sidewall spacers on the sides of the overlying silicon oxide shapes. Formation of silicon nitride spacers on the sides of the STI regions, is followed by deposition of a high k gate insulator layer and of a conductive gate structure, with the conductive gate structure formed self-aligned to the STI regions.

(Figure 15)