

Claims

1. An apparatus for providing an a semiconductor device, comprising:
an analysis module configured to receive information pertaining to the semiconductor device,
wherein the information includes an optimization parameter specification corresponding to an optimization parameter and at least one target parameter corresponding to the optimization parameter, and
wherein the at least one target parameter also corresponds to a physical dimension of the semiconductor device and the physical dimension corresponds to a geometric layout parameter;
a G-function processor coupled to the analysis module,
wherein the G-function processor is configured to receive at least one of the optimization parameter specification, the at least one target parameter, or the geometric layout parameter, and
wherein the G-function processor formulates an ordered relationship representation between two or more of the optimization parameter specification, the at least one target parameter, or the geometric layout parameter and the ordered relationship representation describes a characteristic of the semiconductor device; and
a power cell optimizer coupled to receive the ordered relationship representation from the G-function processor,
wherein the power cell optimizer includes an optimizer module and the optimizer module transforms the ordered relationship representation to correspond to

the optimization parameter and wherein the optimizer module is a multivariate optimizer, the ordered relationship representation is formed so as to be non-monotonic, and wherein the optimization parameter corresponds to a global error minimum in a solution space defined by the ordered relationship representation, and

wherein the optimization parameter corresponds to an improved characteristic of the semiconductor device.

2. The apparatus of Claim 1, wherein the ordered relationship representation is formed to be non-monotonic.

3. The apparatus of Claim 1, wherein the power cell optimizer module transforms at least one target parameter and wherein when a transformed target parameter modifies fabrication of the semiconductor device, the semiconductor device exhibits the improved characteristic.

~~4. The apparatus of Claim 1, wherein the optimizer module is a multivariate optimizer, the ordered relationship representation is formed to be non-monotonic, and wherein the optimization parameter corresponds to a global error minimum in a solution space defined by the ordered relationship representation.~~

~~5.4.~~ The apparatus of Claim 3, wherein the optimizer module is a multivariate optimizer, the ordered relationship representation is formed to be non-monotonic, and wherein

the optimization parameter corresponds to a global error minimum in a solution space defined by the ordered relationship representation.

6.5. The apparatus of Claim 54, further comprising a semiconductor device simulator coupled to the analysis module,

wherein the power cell optimizer communicates at least one of the optimization parameter and the at least one target parameter to the semiconductor device simulator,

wherein the at least one of the optimization parameter and the at least one target parameter correspond to a simulated behavior;

wherein the semiconductor device simulator performs a simulation of the semiconductor device and generates simulation data in accordance with the simulated device behavior; and

wherein the semiconductor device simulator generates a discrete netlist for points in the device layout.

7.6. The apparatus of Claim 65, further comprising a semiconductor device layout generator coupled to receive the simulation data from the semiconductor device simulator and to generate a semiconductor layout representation corresponding to the simulated device behavior having the improved characteristic.

8.7. The apparatus of Claim 76, wherein the semiconductor device comprises a power cell including an LDMOS transistor having an RD_{SON} characteristic, wherein the at least one

target parameter comprises an area of the transistor, and wherein the improved characteristic comprises an RDSon-Area product, wherein an optimized RDSon-Area product is smaller in magnitude than a non-optimized RDSon-Area product.

9.8. A method for designing a semiconductor device, comprising:
receiving at least one target parameter;
receiving an optimization parameter specification corresponding to an optimization parameter;
receiving by a power cell optimizer the optimization parameter specification, and the at least one target parameter;
receiving a G-function corresponding to an ordered relationship representation among the ~~optimizationparameter~~ optimization parameter specification, at least one target parameter, or the at least one geometric layout parameter;
optimizing the optimization parameter specification as a function of the predetermined G-function; and
producing at least one optimized geometric layout parameter (GLP) by the optimizing, wherein the at least one GLP corresponds to an optimized power cell.

9. An apparatus for providing a semiconductor device, comprising:
an analysis module configured to receive information pertaining to the semiconductor device,

wherein the information includes an optimization parameter specification corresponding to an optimization parameter and at least one target parameter corresponding to the optimization parameter, and

wherein the at least one target parameter also corresponds to a physical dimension of the semiconductor device and the physical dimension corresponds to a geometric layout parameter;

a G-function processor coupled to the analysis module,

wherein the G-function processor is configured to receive at least one of the optimization parameter specification, the at least one target parameter, or the geometric layout parameter, and

wherein the G-function processor formulates an ordered relationship representation between two or more of the optimization parameter specification, the at least one target parameter, or the geometric layout parameter and the ordered relationship representation describes a characteristic of the semiconductor device; and

a power cell optimizer coupled to receive the ordered relationship representation from the G-function processor,

wherein the power cell optimizer includes an optimizer module and the optimizer module transforms the ordered relationship representation to correspond to the optimization parameter and wherein the power cell optimizer module transforms at least one target parameter and wherein when a transformed target parameter modifies fabrication of the semiconductor device, the semiconductor device exhibits the improved characteristic; and

wherein the optimization parameter corresponds to an improved characteristic of the semiconductor device.

10. The apparatus of Claim 9, wherein the optimizer module is a multivariate optimizer, the ordered relationship representation is formed to be non-monotonic, and wherein the optimization parameter corresponds to a global error minimum in a solution space defined by the ordered relationship representation.

11. The apparatus of Claim 9, further comprising a semiconductor device simulator coupled to the analysis module,

wherein the power cell optimizer communicates at least one of the optimization parameter and the at least one target parameter to the semiconductor device simulator,

wherein the at least one of the optimization parameter and the at least one target parameter correspond to a simulated behavior,

wherein the semiconductor device simulator performs a simulation of the semiconductor device and generates simulation data in accordance with the simulated device behavior, and

wherein the semiconductor device simulator generates a discrete netlist for points in the device layout.

12. The apparatus of Claim 10, further comprising a semiconductor device layout generator coupled to receive the simulation data from the semiconductor device simulator and to

generate a semiconductor layout representation corresponding to the simulated device behavior
having the improved characteristic.