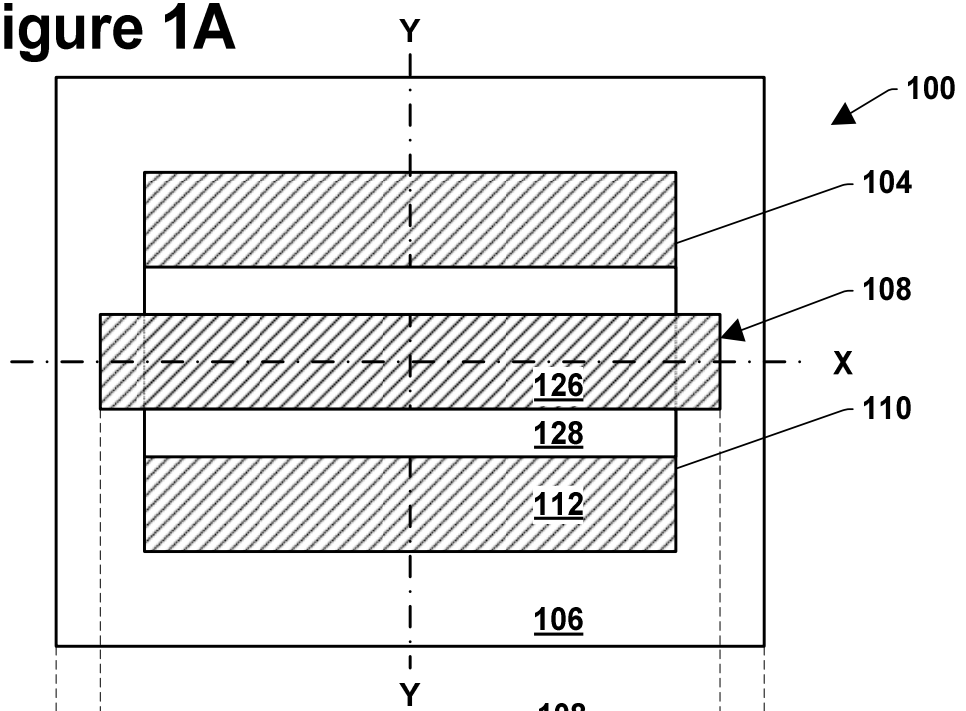
Figure 1A



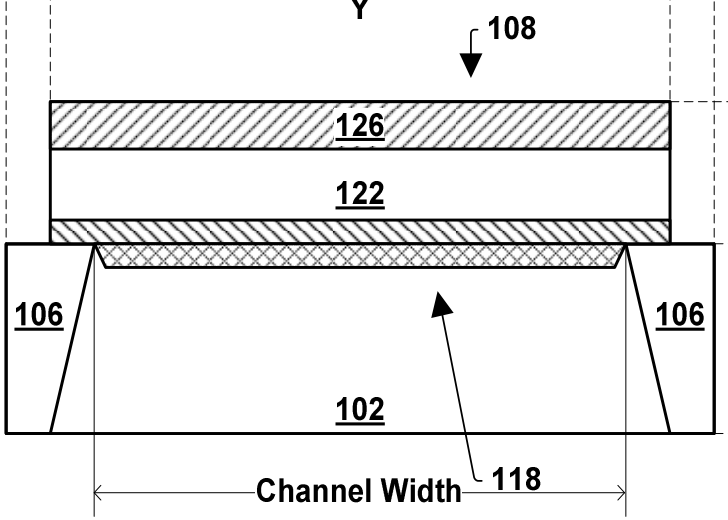


Figure 1B

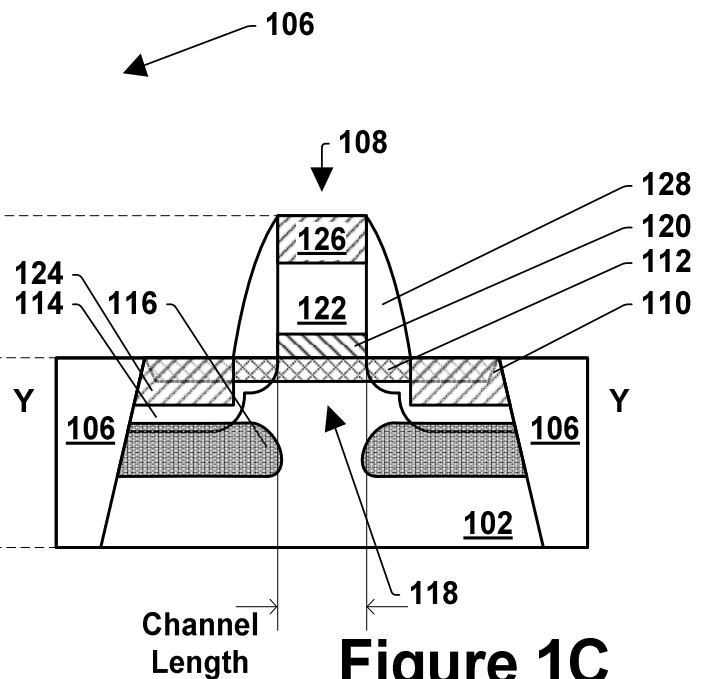


Figure 1C

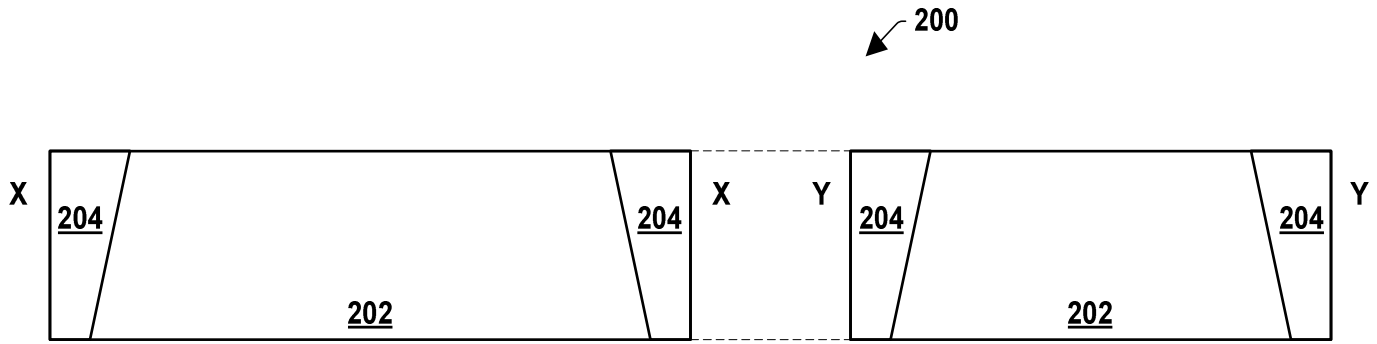


Figure 2A

Figure 2B

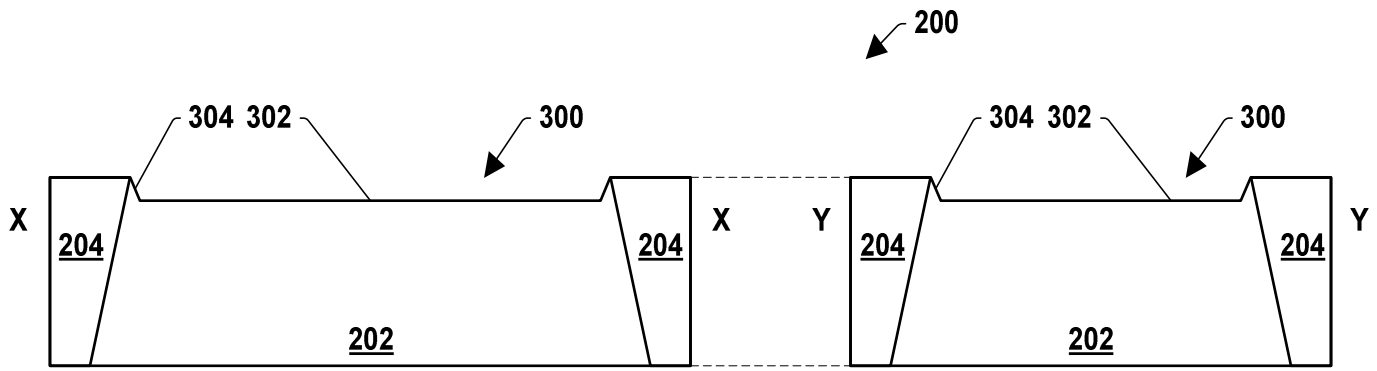


Figure 3A

Figure 3B

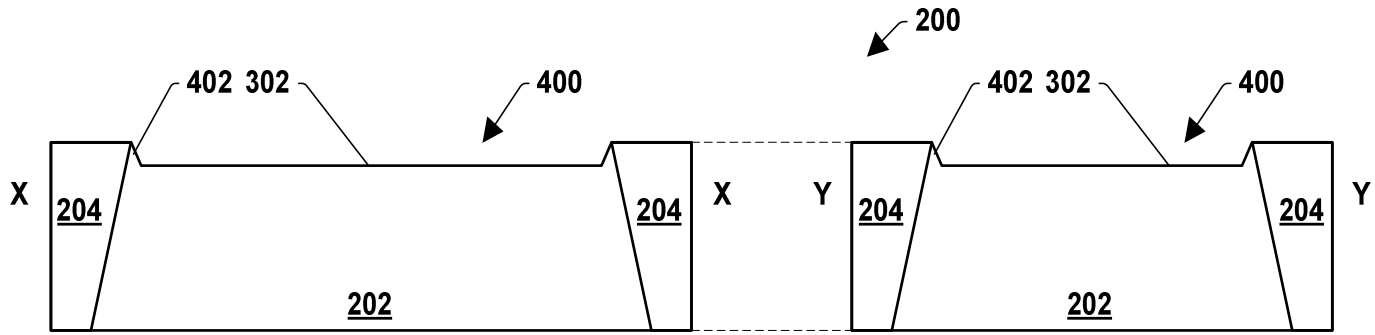


Figure 4A

Figure 4B

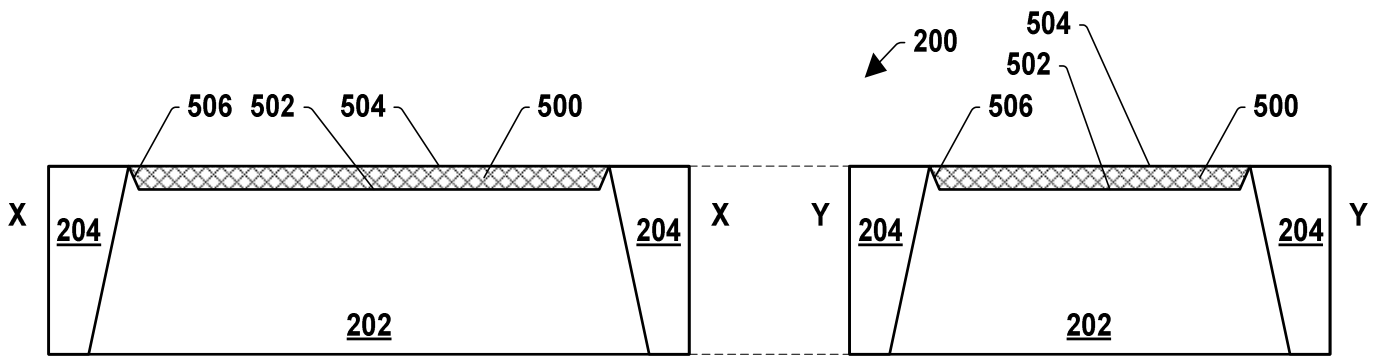


Figure 5A

Figure 5B

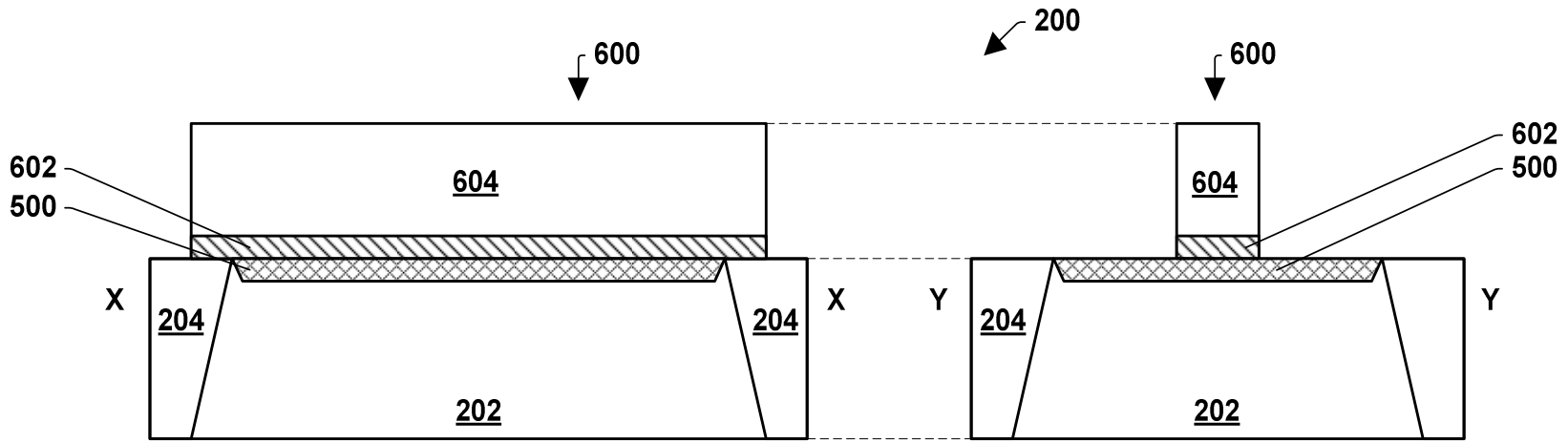


Figure 6A

Figure 6B

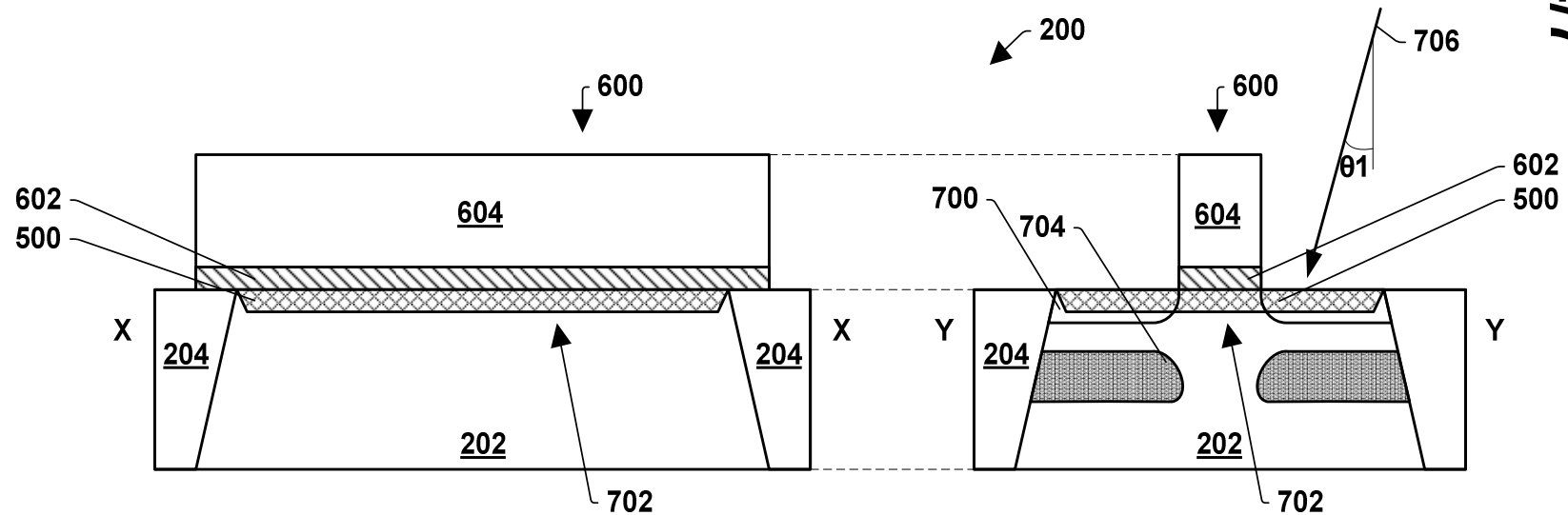


Figure 7A

Figure 7B

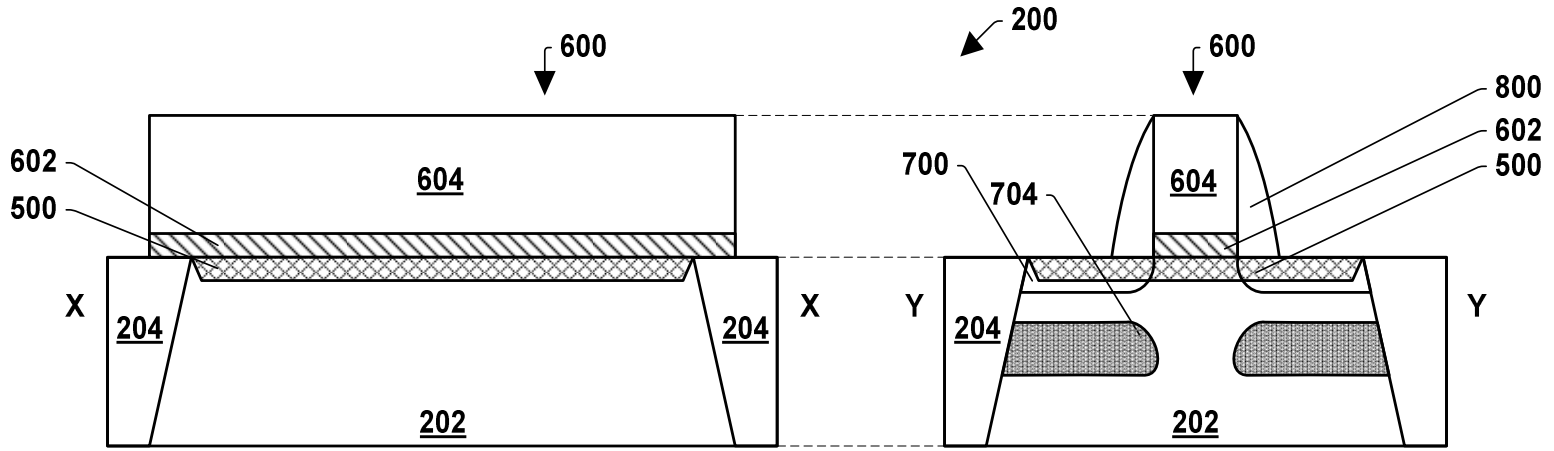


Figure 8A

Figure 8B

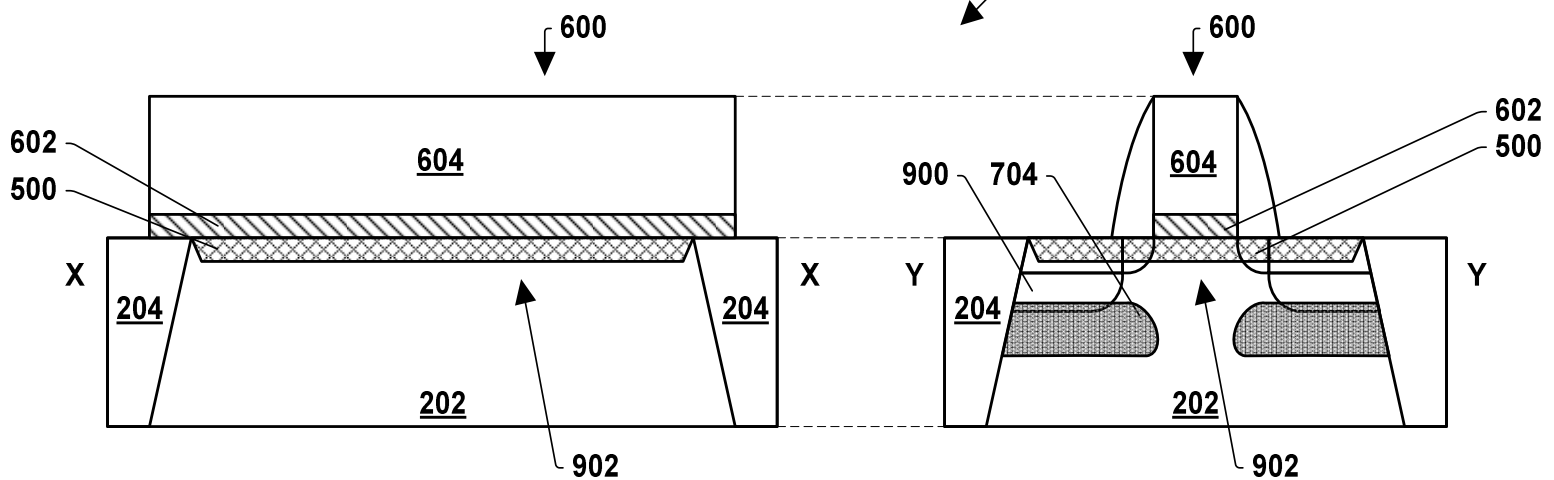


Figure 9A

Figure 9B

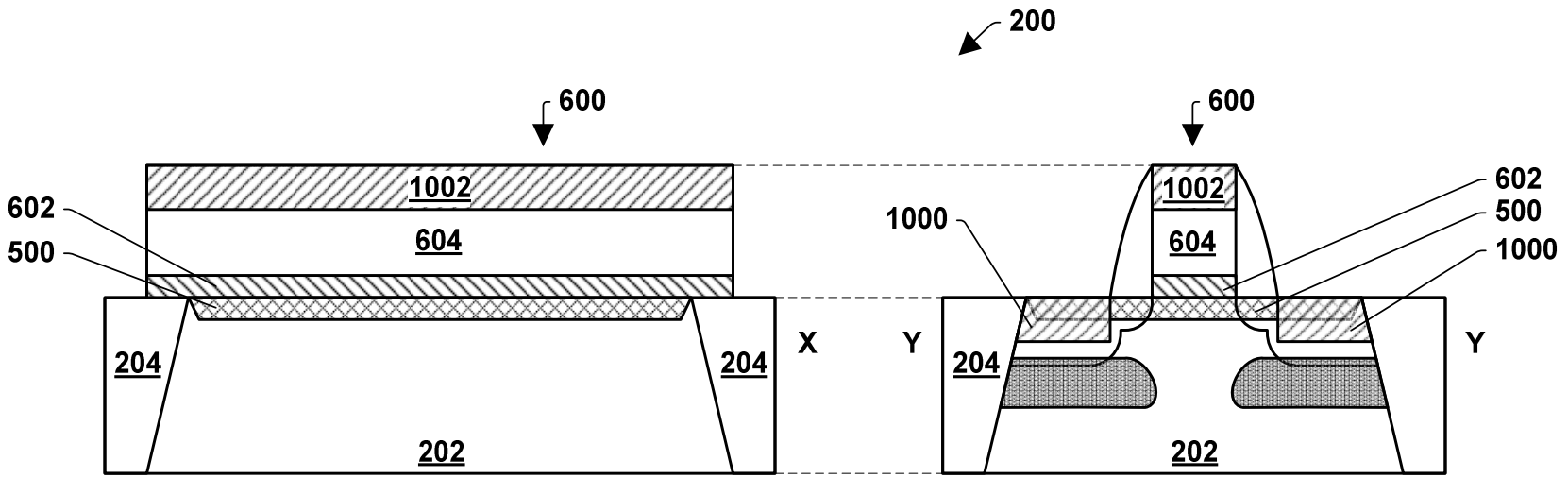


Figure 10A

Figure 10B

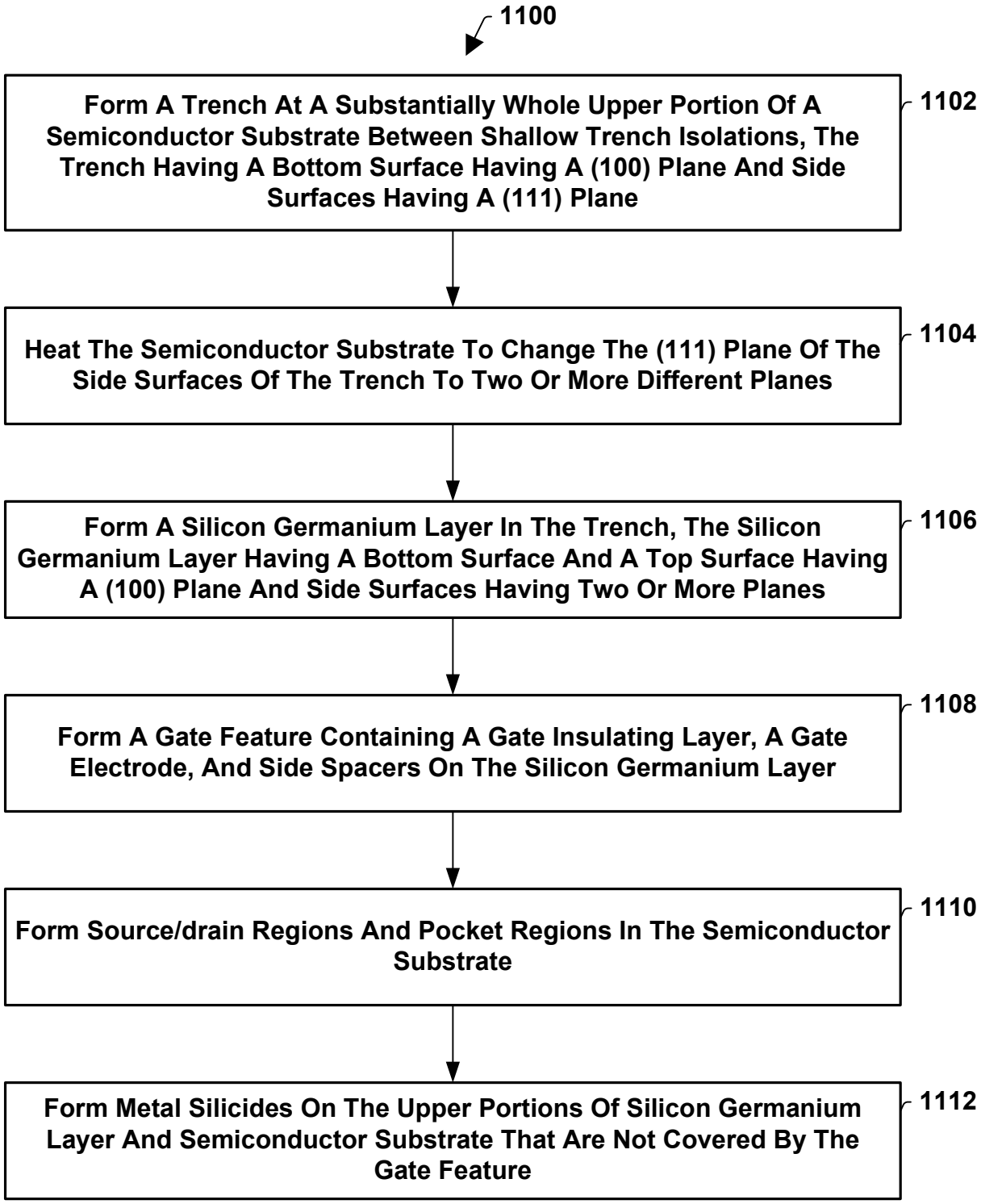

1100
Form A Trench At A Substantially Whole Upper Portion Of A Semiconductor Substrate Between Shallow Trench Isolations, The Trench Having A Bottom Surface Having A (100) Plane And Side Surfaces Having A (111) Plane
1102
Heat The Semiconductor Substrate To Change The (111) Plane Of The Side Surfaces Of The Trench To Two Or More Different Planes
1104
Form A Silicon Germanium Layer In The Trench, The Silicon Germanium Layer Having A Bottom Surface And A Top Surface Having A (100) Plane And Side Surfaces Having Two Or More Planes
1106
Form A Gate Feature Containing A Gate Insulating Layer, A Gate Electrode, And Side Spacers On The Silicon Germanium Layer
1108
Form Source/drain Regions And Pocket Regions In The Semiconductor Substrate
1110
Form Metal Silicides On The Upper Portions Of Silicon Germanium Layer And Semiconductor Substrate That Are Not Covered By The Gate Feature
1112

Figure 11