PACKAGED MICROELECTRONIC DEVICES RECESSED IN SUPPORT MEMBER CAVITIES, AND ASSOCIATED METHODS

TECHNICAL FIELD

[0001] The present disclosure is directed generally toward packaged microelectronic devices, including microelectronic dies, that are recessed in a cavity of a corresponding support member (e.g., a circuit board). The disclosure is also directed to associated methods.

BACKGROUND

[0002] Packaged microelectronic assemblies, such as memory chips, imagers, and microprocessor chips, typically include a microelectronic die mounted to a substrate and encased in a plastic protective covering or encapsulant. The die includes functional features, such as memory cells, processor circuits, and interconnecting circuitry. The die also typically includes bond pads electrically coupled to the functional features. The bond pads are electrically connected to pins or other types of terminals that extend outside the protective covering for connecting the die to busses, circuits, and/or other microelectronic assemblies.

[0003] One approach for carrying a microelectronic die in a package is to support it on an interposer board or other type of circuit board. The interposer board can include a first set of bond pads to which the microelectronic die is electrically connected with wire bonds or solder balls. Conductive traces route electrical signals between the first set of bond pads and a second set of bond pads that are accessible from outside the package encapsulant for connections to other devices.

[0004] Customer demands have resulted in increasing pressure on manufacturers to make the encapsulated microelectronic die packages smaller. In response, some manufacturers have recessed the microelectronic die in the circuit board to reduce the thickness of the resulting package. One approach to recessing the microelectronic die is to (a) form a cavity extending entirely through the circuit board, (b) place a layer of a

removable adhesive across one opening of the cavity, and then (c) temporarily support the die in the cavity with the adhesive while the die is electrically connected to the circuit board. The die is then encapsulated in the cavity, which both secures the die to the circuit board and protects the electrical connections between the die and the circuit board. The adhesive layer is then removed.

[0005] One potential drawback with the foregoing approach is that it requires the use of a removable adhesive layer to temporarily secure the die to the circuit board during manufacture. The operation of first attaching the removable adhesive layer and then detaching the removable adhesive layer can add to the overall flow time required to produce the microelectronic device package. This can in turn reduce the throughput of a package production line, and/or increase the cost of producing such packages.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] Figures 1A-1E are partially schematic side cross-sectional views illustrating a process for forming a support member having a cavity configured to receive a microelectronic device in accordance with an embodiment of the invention.

[0007] Figures 2A-2B are partially schematic, side cross-sectional views illustrating a process for mounting multiple microelectronic devices to a support member in accordance with an embodiment of the invention.

[0008] Figure 3 is a partially schematic, side cross-sectional view of a package having multiple microelectronic devices with different configurations carried by a support member in accordance with another embodiment of the invention.

[0009] Figure 4 is a partially schematic, side cross-sectional view of a package having two microelectronic devices with independent package bond sites, in accordance with yet another embodiment of the invention.

[0010] Figure 5 is a partially schematic, side cross-sectional view of a package having two microelectronic devices and corresponding package bond sites facing in opposing directions.

[0011] Figure 6 is a partially schematic, side cross-sectional view of a package having a single microelectronic device recessed in a cavity formed in a single support member element, in accordance with still another embodiment of the invention.

DETAILED DESCRIPTION

[0012] The present disclosure relates generally to microelectronic device packages, including packages having a support member with a cavity and a microelectronic device carried by a conductive surface of the cavity. For example, a microelectronic device package in accordance with one aspect includes a support member having a cavity with a cavity opening and a closed end opposite the opening, with the closed end having a conductive layer. The package can further include a microelectronic device disposed in the cavity, with the microelectronic device having bond sites that are electrically coupled to the conductive layer. The microelectronic device can further have a first surface and a second surface facing opposite from the first surface, with the second surface facing toward and carried by the conductive layer in the cavity. The presence of the conductive layer at the closed end of the cavity can eliminate the need for a removable adhesive layer at that location during manufacture, and can also provide for electrical connections to the microelectronic device.

[0013] In particular aspects, the support member can include a first support member element having a conductive layer, and a second support member element having another conductive layer. An intermediate element can be positioned between the two support member elements. In further particular embodiments, each of the support member elements can include a circuit board. In still another aspect, the support member can carry multiple microelectronic devices stacked one upon the other. The microelectronic devices can be electrically isolated from each other within the package, or can be electrically coupled to each other within the package. When electrically isolated, each microelectronic device can be coupled to a corresponding set of device bond sites which may be positioned on the same side or on opposite sides of the package.

[0014] Further aspects are directed to methods for packaging a microelectronic device. One such method can include positioning a microelectronic device in a cavity of

a support member. The cavity can have a closed end with a conductive layer, and an opening through which the cavity is accessible. The microelectronic device can have bond sites, a first surface, and a second surface facing opposite from the first surface, with the second surface facing toward and carried by the conductive layer. The method can further include electrically coupling the microelectronic device to the conductive layer. In particular aspects, the microelectronic device can be encapsulated without temporarily supporting the microelectronic device in the cavity with a removable tape layer.

[0015] In particular aspects, the support member can be formed from multiple support member elements. For example, the support member can include a first support member element having a conductive layer and a second support member element also having a conductive layer, and the method can further include attaching the first and second support member elements to each other with an intermediate element. The cavity can be made to extend entirely through the first support member element and the intermediate element, and can extend part-way through the second support member element, for example, to expose the conductive layer of the second support member element.

[0016] In a further aspect, the package can be made to include multiple microelectronic devices. For example, the support members can include first and second conductor layers, and a cavity with the second conductive layer at a closed end of the cavity. A first microelectronic device can be positioned in the cavity, and can have a first surface (with bond sites accessible from the first surface), and a second surface facing opposite from the first surface and positioned against the second conductive layer. A second microelectronic device can be stacked on the first microelectronic device in the cavity, and each microelectronic device can be electrically coupled to at least one of the conductive layers. For example, both microelectronic devices can be electrically coupled to the same conductive layer in one particular arrangement. In another arrangement, the first microelectronic device can be coupled to first package bond sites and the second microelectronic device can be coupled to second package bond sites, with the second package bond sites being electrically isolated from the first package bond sites.

[0017] Many specific details of particular embodiments are set forth in the following description and Figures 1A-6 to provide a thorough understanding of these embodiments. One skilled in the art, however, will understand that the present invention may have additional embodiments, and that the invention may be practiced without several of the details described below.

[0018] Figures 1A-1E illustrate a process for preparing a support member 110 that carries a microelectronic device (e.g., a microelectronic die) in accordance with an embodiment of the invention. Figure 1A illustrates a support member 110 formed from an assembly of initially separate elements. These elements can include a first support member element 120, (referred to as a first element 120) a second support member element 130, (referred to as a second element 130) and an intermediate element 113 (e.g., an adhesive) that joins the first and second elements 120, 130 in a sandwich construction. Each of the first and second elements 120, 130 can include a circuit board. Accordingly, the first element 120 can include a first conductive layer 122 separated from a second conductive layer 123 by an insulating layer 121. The second element 130 can also include a first conductive layer 132 separated from a second conductive layer 133 by an insulating layer 131. The intermediate element 113 can include an epoxy (e.g., an epoxy sheet) or another adhesive material that is sandwiched between the first element 120 and the second element 130. In a particular aspect of this embodiment, the intermediate element 113 can have a thickness T selected to control the overall thickness of the assembled support member 110, as will be described in greater detail below with reference to Figure 1D.

[0019] In Figure 1B, the intermediate element 113 has been attached to the first element 120. The composite of the first element 120 and the intermediate element 113 can undergo an elevated temperature curing process to solidify the bond between these two elements. In other embodiments, the first element 120 and the intermediate element 113 can be attached to each other in a room temperature process.

[0020] Figure 1C illustrates the support member 110 after the formation of a cavity 116 in the elements that form the support member 110. The cavity 116 can include a first cavity portion 124 that extends through the first element 120 and the adjacent intermediate element 113. The cavity 116 can further include a second cavity portion

134 that extends part-way through the second element 130. Accordingly, the second cavity portion 134 can extend through the first conductive layer 132 and the insulating layer 131 of the second element 130, but not through the second conductive layer 133. In an embodiment shown in Figure 1C, the cavity portions 124, 134 are formed in the separate sections of the support member 110 before the sections are joined. Accordingly, a relatively high-speed process (e.g., a punching process) can be used to form the first cavity portion 124. A different process (e.g., an etching process) can be used to form the second cavity portion 134. For example, a two-step etching process can be used to extend the second cavity portion 134 (a) through the first conductive layer 132 and then (b) through the insulating layer 131. An advantage of an embodiment that includes forming the first and second cavity portions 124, 134 separately is that is allows at least the first cavity portion 124 to be formed using a relatively high-speed process. However, in other embodiments, the entire cavity 116 can be formed after the second element 130 is joined to the intermediate element 113, for example, using a series of etching processes.

[0021] Figure 1D illustrates the support member 110 after the second element 130 is joined to the composite formed by the first element 120 and the intermediate element 113. This attachment process can be generally similar to the process used to attach the first element 120 to the intermediate element 113. Once attached, the cavity 116 has an opening 117 and a closed end 118 opposite the opening 117. The closed end 118 is bounded by a conductive material, in this case, the second conductive layer 133 of the second element 130. The overall height H of the support member 110 can be controlled by selecting the thickness T of the intermediate element 113, once the thicknesses of the first and second elements 120, 130 have been established. In some embodiments, the overall height H can also be controlled by selecting the thicknesses of the first element 120 and/or the second element 130. The overall height H of the support member 110 can determine at least in part the depth D of the cavity 116, which in turn can determine the size and/or number of microelectronic devices that will fit in the cavity 116.

[0022] The first conductive layer 122 and/or the second conductive layer 133 can be patterned using existing etching techniques to form two sets of bond sites. For

example, internal bond sites 103 can be formed in the first conductive layer 122 and can be positioned to be electrically connected to a microelectronic device that is subsequently positioned in the cavity 116. Package bond sites 101 can be formed in the second conductive layer 133 and can be positioned for coupling to external devices (not shown in Figure 1D). Conductive vias 111 can be formed in the support member 110 (e.g., using existing etching and material deposition techniques) to connect the internal bond sites 103 to the package bond sites 101. The conductive vias 111 can accordingly provide signal paths between the first conductive layer 122 and the second conductive layer 133, and between the subsequently positioned microelectronic device and external devices.

[0023] Figure 1E illustrates the support member 110 after a solder mask 102 or other appropriate insulating layer has been disposed on the first conductive layer 122 and the second conductive layer 133. The solder mask 102 can be selectively etched away and/or formed in a manner so as to leave the internal bond sites 103 at the first conductive layer 122, and the corresponding package bond sites 101 at the second conductive layer 133 exposed for subsequent electrical connections.

[0024] Figure 2A illustrates the support member 110 after a first microelectronic device 140a has been positioned in the cavity 116. In this particular case, the support member 110 is configured to carry stacked microelectronic devices, as will be described in greater detail below with reference to 2B. The first microelectronic device 140a can include a microelectronic die, for example, a memory chip or a processor chip. Accordingly, the first microelectronic device 140a can include memory cells, capacitors, processor circuits and/or other functional internal microelectronic features.

[0025] The first microelectronic device 140a can have a first surface 142 facing outwardly toward the cavity opening 117 and a second surface 143 facing toward the closed end 118 of the cavity 116. Accordingly, the second surface 143 can be carried by the second conductive layer 133. In at least some embodiments, a thin die support adhesive 108 or adhesive layer is used to attach the first microelectronic device 140a to the second conductive layer 133. For example, the adhesive 108 can include an adhesive paste or die attach film having a thickness of from about 10 μm to about 25 μm. The adhesive 108 can be electrically insulating, or electrically conductive. For

example, if the second surface 143 of the first microelectronic device includes a conductive ground plane, a conductive adhesive can be used to ground the device 140a to the second conductive layer 133. The second conductive layer 133 can be patterned to isolate the grounding portion of the layer from the signal-carrying bond pads 107.

[0026] The first microelectronic device 140a can include multiple device bond sites 141 accessible from the first surface 142. The device bond sites 141 can be connected to the corresponding internal bond sites 103 with wire bonds 106 or another suitable electrical coupling. As will be clear to one of ordinary skill in the relevant art, the first microelectronic device 140a can include multiple device bond sites 141 extending perpendicular to the plane of Figure 2A, which are coupled to corresponding multiple internal bond sites 103, also extending perpendicular to the plane of Figure 2A. Each internal bond site 103 can be electrically coupled to a corresponding package bond site 101 with a via 111, as described above. Each package bond site 101 can include a bond pad 107 or other appropriate provision for connecting the package 100 to external devices. The bond pads 107 can be arranged in a ball grid array, a land grid array, or another appropriate pattern, depending upon the particular use to which the package is intended to be put. Solder balls (not shown in Figure 2B) can be used to electrically couple the bond pads 107 to external devices.

[0027] Figure 2B illustrates the package 100 after additional microelectronic devices (including a second microelectronic device 140b and a third microelectronic device 140c) are stacked on the first microelectronic device 140a and attached with inter-die adhesive layers 105. These layers 105 can include epoxy, and can be thicker (e.g., 100 μm) than the die support adhesive 108. Each of the microelectronic devices 140a-140c can be connected with wire bonds 106 to corresponding internal bond sites 103. In one aspect of this embodiment, the microelectronic devices 140a-140c can share internal bond sites 103. For example, a given device bond site 141a of the first microelectronic device 140a can be coupled to an internal bond site 103, and the corresponding device bond sites 141b, 141c of the second microelectronic device 140b and the third microelectronic device 140c, respectively, can be coupled to the same internal bond site 103. This arrangement can be particularly suitable when the first, second and third microelectronic devices 140a-140c have identical or otherwise

compatible configurations. When the microelectronic device configurations are identical, each successive microelectronic device completely overlays the microelectronic device beneath. Accordingly, the wire bonds 106 for a given microelectronic device are typically connected to the corresponding internal bond site 103 before the next microelectronic device is stacked on top. In other arrangements, such as that described below with reference to Figure 3, the microelectronic devices may be stacked prior to connecting wire bonds to each device. In any of these embodiments, the wire bonds 106 and the microelectronic devices themselves can then be protected with an encapsulant 104.

[0028] One feature of an embodiment of the arrangement shown in Figure 2B is that the first microelectronic device 140a is supported by the second conductive layer 133, both during manufacture and after the package 100 is completed. One expected benefit of this arrangement is that it does not require a removable tape layer to carry the first microelectronic device 140a (and any devices stacked on top of it) during manufacture, and such a tape layer need not subsequently be removed. Accordingly, the process for forming the package 100 (once the support member 110 has been manufactured) can be reduced when compared with existing processes that include the use of a removable tape layer during the package formation process.

[0029] Another potential benefit of the second conductive layer 133 is that it can transfer additional heat away from the package 100, and in particular, away from the first microelectronic device 140a. More specifically, the electrically conductive layer of the closed end of the cavity in the support member conducts heat away from the first microelectronic device 140a. Increasing the amount of heat transferred away from the package 100 can increase the expected lifetime of the package 100, and can reduce the likelihood for package failures. Increasing the heat transfer rate is particularly important for high-performance devices that operate at higher speeds. This feature can also allow the package to be used in harsher thermal environments.

[0030] Still another expected benefit of the second conductive layer 133 is that it can protect the second surface 143 of the first microelectronic device 140a. In other existing packages, the second surface 143 can remain exposed after the temporary tape layer described above has been removed. In some cases, the exposed second

surface 143 may increase the likelihood for damage to the first microelectronic device 140a. In other existing arrangements, an additional protective material is placed against the exposed second surface 143. However, an embodiment of the current method can provide such protection without the additional step of adding a protective layer.

[0031] Yet another expected benefit of the foregoing arrangement is that the first and second elements 120, 130 can be formed using existing printed circuit boards having the structure shown in Figure 1A, along with existing processing techniques for attaching the printed circuit boards to each other, patterning the conductive layers of the printed circuit boards, and forming vias to connect the conductive layers. Accordingly, embodiments of the foregoing method can be implemented without the need for significantly tailored and/or specialized manufacturing techniques.

[0032] Figures 3-6 illustrate device packages having arrangements in accordance with further embodiments of the invention, all of which use some or all of the techniques and arrangements described above with reference to Figures 1A-2B. For example, Figure 3 illustrates a package 300 having a support member 310 generally similar to the support member 110 shown in Figure 1E. The support member 310 carries first, second and third microelectronic devices 340a, 340b, and 340c, each of which may have a different size and/or configuration. In one aspect of this arrangement, the first microelectronic device 340a has a larger planform footprint than the second microelectronic device 340b, which in turn has a larger planform footprint than the third microelectronic device 340c. Because the device bond sites 341a-341c of each microelectronic device 340a-340c are laterally offset from the device bond sites of the microelectronic device immediately above, all three devices 340a-340c can be stacked on each other prior to wire bonding any of the microelectronic devices 340a-340c to corresponding internal bond sites 303. An advantage of this arrangement is that it can reduce the time required to form the package 300 because multiple similar steps can be performed sequentially at one processing station without moving the package 300 back and forth multiple times between processing stations. For example, all three microelectronic devices 340a-340c can be stacked while the package remains at a stacking station, and all three microelectronic devices 340a-340c can be wire bonded while the package 300 remains at a wire bonding station.

[0033] In one aspect of an embodiment shown in Figure 3, similar, identical, or otherwise related device bond sites 341 can be coupled to a corresponding single internal bond site 303. In other embodiments, the package 300 may include multiple internal bond sites 303, all at the first conductive layer 322, and each dedicated to a corresponding device bond site 341 of one of the microelectronic devices 340a-340c. Further details of another arrangement in which individual microelectronic devices may be coupled to corresponding individual bond sites are described below with reference to Figures 4 and 5.

[0034] Figure 4 illustrates a package 400 that includes a support member 410 carrying a first microelectronic device 440a, and a stacked second microelectronic device 440b. The first microelectronic device 440a can be coupled to first package bond sites 401a, and the second microelectronic device 440b can be coupled to second package bond sites 401b that are electrically isolated from the first package bond sites 401a. Accordingly, electrical signals can be sent to and from the first microelectronic device 440a independently of signals sent to and from the second microelectronic device 440b.

[0035] In one aspect of an embodiment shown in Figure 4, the support member 410 can include a first conductive layer 422 and a second conductive layer 433. The first microelectronic device 440a can be electrically coupled to first internal bond sites 403a located at the second conductive layer 433, e.g., with wire bonds 406 or other suitable couplers. The second conductive layer 433 can be patterned to provide an electrical signal path between the first internal bond sites 403a and corresponding first package bond sites 401a, also located at the second conductive layer 433. The second microelectronic device 440b can be electrically coupled to second internal bond sites 403b located at the first conductive layer 422. The first conductive layer 422 can be patterned and coupled with appropriate vias 411 to corresponding second package bond sites 401b located at the second conductive layer 433. The electrical signal path between the first package bond sites 401a and the first microelectronic device 440a can be electrically isolated from the electrical signal path between the second package bond sites 401b and the second microelectronic device 440b. Accordingly, signals may be transmitted to and from the first microelectronic device 420a independently of signals

transmitted to and from the second microelectronic device 420b. A similar arrangement can be used to provide independent signal paths to more (e.g., three) microelectronic devices carried by a single support member.

[0036] Figure 4 also illustrates (in dashed lines) another embodiment in which electrical connections to the first microelectronic device 440a may be made with solder balls 409. The solder balls 409 can be positioned between the second conductive layer 433 and bond sites that are accessible from a downwardly facing second surface 443 of the first microelectronic device 440a, rather than the upwardly facing first surface 442. The second conductive layer 433 can both carry the first microelectronic device 440a and provide electrical signal paths to the first microelectronic device 440a.

[0037] In one aspect of an arrangement shown in Figure 4, the first package bond sites 401a and the second package bond sites 401b are all accessible from the same side (e.g., the downwardly facing side) of the package 400. Figure 5 illustrates a package 500 arranged so that the package bond sites for different dies within the package 500 are accessible from different directions. In particular, the package 500 can include a support member 510 having a first conductive layer 522 and a second conductive layer 533. A first microelectronic device 540a can be electrically connected with wire bonds to first package bond sites 501a located at the second conductive layer 533. A second microelectronic device 540b can be connected with wire bonds to second package bond sites 501b located at the first conductive layer 522. As is shown in Figure 5, the first package bond sites 501a and the second package bond sites 501b are accessible from opposite sides of the package 500.

[0038] The arrangements described above with reference to Figures 1A-5 illustrate support members formed from multiple elements and configured to carry multiple microelectronic devices. In other embodiments, the support member may be formed from a single element, and/or may carry only a single microelectronic device. Figure 6 illustrates a package 600 that includes both a single-element support member 610 and a single microelectronic device 640. In one aspect of this arrangement, the support member 610 can include a single support member element 620 (e.g., a single circuit board) having a first conductive layer 632, a second conductive layer 633, and an insulating layer 621 between the first and second conductive layers 622, 633. Vias 611

can provide for electrical coupling between the two conductive layers 622, 633. A cavity 616 can be formed in the support member 610 using an etching technique or another appropriate technique. The microelectronic device 640 can be positioned in the cavity 610 so that it is placed against the second conductive layer 633. The microelectronic device 640 can then be coupled to corresponding internal bond sites 603 with wire bonds 606 or other appropriate electrical couplings. In a particular aspect of this embodiment, the microelectronic device 640 can be shorter than the walls of the cavity 616, so as not to project above the cavity 616. In other embodiments, the microelectronic device 640 can project above the cavity 616, so long as a corresponding encapsulant 604 can still be positioned to protect the wire bonds 606 and the connections between the wire bonds and both the microelectronic device 640 and the support member 610.

[0039] An advantage of an embodiment of the single-element support member 610 shown in Figure 6 is that it may be simpler and therefore faster and/or less expensive to manufacture than are multi-element support members. The single-element support member may, in at least some embodiments, be thinner than a multi-element support member, and may therefore be particularly appropriate for packages having thin single dies or thin multi-die stacks. Conversely, embodiments of the multi-element support members may be particularly appropriate for thicker dies and/or die stacks.

[0040] Although advantages associated with certain embodiments of the invention have been described in the context of those embodiments, other embodiments may also exhibit such advantages. For example, at least some advantages described above with reference to Figures 1A-2B may apply as well to embodiments described with reference to Figures 3-6. Additionally, none of the foregoing embodiments need necessarily exhibit such advantages for fall within the scope of the invention. Aspects of certain embodiments described above may be combined or eliminated in other embodiments. For example, certain aspects described in detail with reference to Figures 1A-2B may be included in embodiments shown in Figures 3-6.

[0041] From the foregoing, it will be appreciated that specific embodiments of the invention have been described herein for purposes of illustration, but that various modifications may be made without deviating from the scope of the invention. For

example, the microelectronic devices and corresponding support members can have configurations other than those shown in the Figures. In particular embodiments, electrical couplings other than the wire bonds may be used to electrically couple the microelectronic devices to bond sites internal to the package, and/or couplings other than solder balls may be used to connect the resulting package to external devices. Couplings that include any combination of wire bonds, vias, patterned layers, and/or other features may be used to electrically couple microelectronic devices to externally-accessible package bond sites. Accordingly, the invention not limited except as by the appended claims.

CLAIMS

I/We claim:

[c1] 1. A method for packaging a microelectronic device, comprising:

positioning a microelectronic device in a cavity of a support member, the cavity having a closed end with an electrically conductive layer and an opening through which the cavity is accessible, the microelectronic device having bond sites, a first surface, and a second surface facing opposite from the first surface, the second surface facing toward and carried by the conductive layer; and

electrically coupling bond sites of the microelectronic device to the conductive layer.

[c2] 2. The method of claim 1, further comprising attaching the second surface of the microelectronic die to the conductive layer with an adhesive disposed between the second surface and the conductive layer.

[c3] 3. The method of claim 2, further comprising encapsulating both the microelectronic device and the adhesive while the microelectronic device is in the cavity and supported by the conductive layer.

[c4] 4. The method of claim 1, further comprising supporting the microelectronic device with the conductive layer and encapsulating the microelectronic device while the microelectronic device is in the cavity and supported by the conductive layer.

[c5] 5. The method of claim 1, further comprising encapsulating the microelectronic device in the cavity without temporarily supporting the microelectronic device in the cavity with a removable tape layer.

[c6] 6. The method of claim 1 wherein electrically coupling the microelectronic device to the conductive layer includes connecting the microelectronic device to an intermediate conductive structure that is in turn electrically coupled to the conductive layer.

[c7] 7. The method of claim 1, further comprising forming the cavity in the support member.

[c8] 8. The method of claim 1 wherein positioning the microelectronic device in the cavity of the support member includes positioning the microelectronic device in the cavity of a circuit board.

[c9] 9. The method of claim 1 wherein positioning the microelectronic device in the cavity of the support member includes positioning the microelectronic device in the cavity of a circuit board having a first conductive layer, a second conductive layer, and an insulating layer between the first and second conductive layers, and wherein the second surface of the microelectronic device faces toward the second conductive layer.

[c10] 10. The method of claim 1 wherein the support member includes a first support member element having a first conductive layer and a second support member element having a second conductive layer, and wherein the method further comprises attaching the first and second support member elements prior to positioning the microelectronic device in the cavity of the support member, further wherein the second surface of the microelectronic device faces toward the second conductive layer.

[c11] 11. The method of claim 10, further comprising forming a via to electrically connect the first and second conductive layers.

[c12] 12. The method of claim 10 wherein attaching the first and second support member elements includes:

attaching the first support member element to an intermediate element; and

attaching the second support member element to the intermediate element, with the intermediate element positioned between the first and second support member elements.

[c13] 13. The method of claim 10 wherein attaching the first and second support member elements includes:

attaching the first support member element to an intermediate element;

forming a first portion of the cavity extending entirely through the first support member element and the intermediate member;

attaching the second support member element to the intermediate element, with the intermediate element positioned between the first and second support member elements; and

forming a second portion of the cavity extending only partially through the second support member element.

[c14] 14. The method of claim 13 wherein forming the second portion of the cavity includes forming the second portion of the cavity before attaching the second support member element to the intermediate element.

[c15] 15. The method of claim 13 wherein forming the second portion of the cavity includes forming the second portion of the cavity after attaching the second support member element to the intermediate element.

[c16] 16. The method of claim 1 wherein the microelectronic device is a first microelectronic device, and wherein the method further includes stacking a second microelectronic device on the first microelectronic device in the cavity.

[c17] 17. The method of claim 16, further comprising electrically coupling both the first and second microelectronic devices to the conductive layer.

[c18] 18. The method of claim 1 wherein electrically coupling the microelectronic device to the conductive layer includes connecting a wire bond between the microelectronic device and the support member.

[c19] 19. The method of claim 1 wherein the bond sites are accessible from the first surface of the microelectronic device, and wherein electrically coupling the microelectronic device includes coupling wire bonds to the bond sites while the microelectronic device is in the cavity.

[c20] 20. The method of claim 1 wherein the conductive layer is electrically coupled to package bond sites, and wherein the method further comprises:

encapsulating the microelectronic device in the cavity; and

providing access to the package bond sites for coupling to external devices after encapsulating the microelectronic device.

[c21] 21. A method for packaging a microelectronic device, comprising:

positioning a microelectronic device in a cavity of a support member, the cavity having a closed end with a conductive layer and an opening through which the cavity is accessible, the microelectronic device being carried by the conductive layer;

electrically coupling the microelectronic device to the conductive layer; and

encapsulating the microelectronic device while the microelectronic device is in the cavity and supported by the conductive layer, without temporarily supporting the microelectronic device in the cavity with a removable tape layer.

[c22] 22. The method of claim 21, further comprising attaching the microelectronic die to the conductive layer with an adhesive disposed between the microelectronic die and the conductive layer.

[c23] 23. The method of claim 21 wherein electrically coupling the microelectronic device to the conductive layer includes connecting the microelectronic device to an intermediate conductive structure that is in turn electrically coupled to the conductive layer.

[c24] 24. The method of claim 21, further comprising forming the cavity in the support member.

[c25] 25. The method of claim 21 wherein positioning the microelectronic device in the cavity of the support member includes positioning the microelectronic device in the cavity of a circuit board having a first conductive layer, a second conductive layer, and an insulating layer between the first and second conductive layers, and wherein the microelectronic device is carried by the second conductive layer.

[c26] 26. The method of claim 21 wherein the support member includes a first support member element having a first conductive layer and a second support member element having a second conductive layer, and wherein the method further comprises attaching the first and second support member elements prior to positioning the microelectronic device in the cavity of the support member, further wherein the microelectronic device is carried by the second conductive layer.

[c27] 27. A method for packaging multiple microelectronic devices, comprising:

attaching a first support member element and a second support member element, the first support member element having a first conductive layer, the second support member element having a second conductive layer;

forming a cavity extending entirely through the first support member element and partially through the second support member element, with the second conductive layer at a closed end of the cavity;

positioning a first microelectronic device in the cavity, the first microelectronic device having a first surface with bond sites accessible from the first surface, the microelectronic device further having a second surface facing opposite from the first surface, the second surface facing toward and carried by the second conductive layer;

stacking a second microelectronic device on the first microelectronic device in the cavity; and

electrically coupling each of the microelectronic devices to at least one of the conductive layers.

[c28] 28. The method of claim 27 wherein attaching the first and second support member elements includes:

attaching the first support member element to an intermediate element; and

attaching the second support member element to the intermediate element, with the intermediate element positioned between the first and second support member elements.

[c29] 29. The method of claim 27 wherein forming the second portion of the cavity includes forming the second portion of the cavity before attaching the second support member element to the intermediate element.

[c30] 30. The method of claim 27 wherein forming the second portion of the cavity includes forming the second portion of the cavity after attaching the second support member element to the intermediate element.

[c31] 31. The method of claim 27 wherein electrically coupling each of the microelectronic devices includes electrically coupling both microelectronic devices to the same conductive layer.

[c32] 32. The method of claim 27 wherein electrically coupling each of the microelectronic devices includes electrically coupling the first microelectronic device to first package bond sites at the second conductive layer and electrically coupling the second microelectronic device to second package bond sites at the second conductive layer, the second package bond sites being electrically isolated from the first package bond sites.

[c33] 33. The method of claim 27 wherein electrically coupling each of the microelectronic devices includes electrically coupling the first microelectronic device to first package bond sites and electrically coupling the second microelectronic device to second package bond sites, the second package bond sites being electrically isolated from the first package bond sites.

[c34] 34. The method of claim 27, further comprising stacking a third microelectronic device on the second microelectronic device in the cavity.

[c35] 35. The method of claim 27, further comprising selecting the first and second microelectronic devices to have at least approximately the same shape and configuration.

[c36] 36. The method of claim 27, further comprising selecting the first and second microelectronic devices to have at least approximately the same shape and configuration.

[c37] 37. A microelectronic device package, comprising:

a support member having a cavity with an opening, a closed end opposite the opening, and a conductive layer at the closed end; and

a microelectronic device disposed in the cavity, the microelectronic device having bond sites electrically coupled to the conductive layer, the microelectronic device further having a first surface and second

surface facing opposite from the first surface, the second surface facing toward and carried by the conductive layer in the cavity.

[c38] 38. The package of claim 37, further comprising an adhesive attached between the second surface of the microelectronic device and the conductive layer.

[c39] 39. The package of claim 37 wherein the second surface of the microelectronic device is not exposed.

[c40] 40. The package of claim 37 wherein the microelectronic device is connected to an intermediate conductive structure that is in turn electrically coupled to the conductive layer.

[c41] 41. The package of claim 37 wherein the cavity is deeper than a corresponding dimension of the support member.

[c42] 42. The package of claim 37 wherein the support member includes a circuit board.

[c43] 43. The package of claim 37 wherein the support member includes a circuit board having multiple conductive layers separated by at least one insulating layer.

[c44] 44. The package of claim 37 wherein the support member includes a first support member element having a first conductive layer and a second support member element having a second conductive layer, and wherein the microelectronic device is carried by the second conductive layer.

[c45] 45. The package of claim 44 wherein the first and second support member elements are attached to an intermediate element positioned between the first and second support member elements.

[c46] 46. The package of claim 44, further comprising an electrically conductive via electrically connected between the first and second conductive layers.

[c47] 47. The package of claim 44 wherein the cavity extends entirely through the first support member element and extends only partially through the second support member element.

[c48] 48. The package of claim 37 wherein the microelectronic device is a first microelectronic device, and wherein the package further comprises a second microelectronic device stacked on the first microelectronic device in the cavity.

[c49] 49. The package of claim 48, wherein both the first and second microelectronic devices are electrically coupled to the conductive layer.

[c50] 50. The package of claim 37 wherein the microelectronic device is electrically coupled to the conductive layer with a wire bond.

[c51] 51. A microelectronic device package, comprising:

a support member having a cavity with an opening, a closed end opposite the opening, and a conductive layer at the closed end, the support member including:

a first support member element having a first aperture extending through it; and

a second support member element attached to the first support member element and having a second aperture extending partially though it, the first and second apertures being axially aligned to form the cavity;

a first microelectronic device disposed in the cavity, the first microelectronic device having a first surface with bond sites accessible from the first surface and electrically coupled to the conductive layer, the microelectronic device further having a second surface facing

opposite from the first surface, the second surface facing toward and carried by the conductive layer in the cavity; and

a second microelectronic device stacked on the first microelectronic device.

[c52] 52. The package of claim 51 wherein the first and second microelectronic devices are electrically coupled to each other.

[c53] 53. The package of claim 51, further comprising:

first package bond sites positioned to couple the package to external devices, the first package bond sites being electrically coupled to the first microelectronic device via a first signal path; and

second package bond sites positioned to couple the package to external devices, the second package bond sites being electrically coupled to the second microelectronic device via a second signal path that is electrically isolated from the first signal path.

[c54] 54. The package of claim 51, further comprising:

first package bond sites positioned to couple the package to external devices, the first package bond sites being electrically coupled to the first microelectronic device; and

second package bond sites positioned to couple the package to external devices, the second package bond sites being electrically coupled to the second microelectronic device and being located at the same conductive layer as the first package bond sites.

[c55] 55. The package of claim 51 wherein the first and second package bond sites are accessible from the same side of the package.

[c56] 56. The package of claim 51 wherein the first and second package bond sites are accessible from the opposite sides of the package.

[c57] 57. The package of claim 51, further comprising an intermediate element positioned between the first and second support member elements.

[c58] 58. The package of claim 51 wherein the conductive layer is the second of two conductive layers of the support member, the second conductive layer being a part of the second support member element, and a first conductive layer being a part of the first support member element, and wherein the first microelectronic device is connected with wire bonds to the second conductive layer, further wherein the second microelectronic device is connected with wire bonds to the second first conductive layer.

[c59] 59. The package of claim 51 wherein the first and second microelectronic devices are electrically coupled to each other.

[c60] 60. The package of claim 51, further comprising a third microelectronic device stacked on the second microelectronic device in the cavity.

[c61] 61. The package of claim 51, wherein the first and second microelectronic devices have at least approximately the same shape and configuration.

[c62] 62. The package of claim 51, wherein the first and second microelectronic devices have different shapes, configurations, or both.