single-crystal semiconductor layer, a second electrically insulating layer, wherein the second electrically insulating layer has a thickness comprised between 10 nm to 30 nm, and a second single-crystal semiconductor layer;

- forming trenches from the surface of said substrate, to the first electrically insulating layer, so as to form at least one fin,

- in each fin, forming a channel of a first transistor in the first semiconductor layer and a channel of a second transistor of opposite type to the first transistor in the second semiconductor layer,

the formation of the double semiconductor-on-insulator substrate comprising:

- a first layer-transfer step comprising forming a weakened zone in a first donor substrate by implantation of atomic species, the first donor substrate is bonded to the carrier substrate, the first electrically insulating layer being at a bonding interface between the first donor substrate and the carrier substrate, and the first donor substrate is detached along the weakened zone in order to transfer the first electrically insulating layer and the first single-crystal semiconductor layer to the carrier substrate, so as to form a first semiconductor-on-insulator substrate, said first layer-transfer step comprising a heat treatment at a sufficiently high temperature to smooth the first single-crystal semiconductor layer that is transferred onto the carrier substrate to a roughness lower than 0.1 nm RMS,

- after said heat treatment, a second layer-transfer step comprising forming a weakened zone in a second donor substrate by implantation of atomic species, the second donor substrate is bonded to the first single-crystal semiconductor layer, the second electrically insulating layer being at a bonding interface between the second donor substrate and the first single-crystal semiconductor layer, and the second donor substrate is detached along the weakened zone in order to transfer the second electrically insulating layer and the second single-crystal semiconductor layer to the first single-crystal semiconductor layer of the first semiconductor-on-insulator substrate.

According to advantageous but optional features of this process, which may be implemented alone or in combination when this is technically appropriate:

- the trenches are formed by etching, the first electrically insulating layer forming a stop layer for said etching;

- the thickness of the first and second single-crystal semiconductor layers is comprised between 25 and 40 nm;

- the thickness of the second electrically insulating layer is comprised between 10 and 30 nm;

- the smoothing heat treatment of the first single-crystal semiconductor layer is carried out at a temperature comprised between 1000 and 1200°C, for a time comprised between 10 and 120 minutes;

- the process further comprises a heat treatment for finishing the second single-crystal semiconductor layer at a temperature comprised between 1100 and 1250°C, carried out for a time shorter than one minute.

The CFET device thus formed comprises a carrier substrate and at least one fin extending from the carrier substrate, in which fin two superposed field-effect transistors of opposite types are arranged, said device being characterized in that each fin comprises, starting from the carrier substrate:

- a first electrically insulating layer;
- a first single-crystal semiconductor layer, forming the channel of a first transistor;
- a second electrically insulating layer;

CLAIMS

1. A process for fabricating a CFET device, wherein it comprises:

- forming a double semiconductor-on-insulator substrate comprising, in succession, from its base to its surface: a carrier substrate, a first electrically insulating layer, a first single-crystal semiconductor layer, a second electrically insulating layer, wherein the second electrically insulating layer has a thickness comprised between 10 nm and 30 nm, and a second single-crystal semiconductor layer;

- forming trenches from the surface of said substrate, to the first electrically insulating layer, so as to form at least one fin,

- in each fin, forming a channel of a first transistor in the first semiconductor layer and a channel of a second transistor of opposite type to the first transistor in the second semiconductor layer,

the formation of the double semiconductor-on-insulator substrate comprising:

- a first layer-transfer step comprising forming a weakened zone in a first donor substrate by implantation of atomic species, the first donor substrate is bonded to the carrier substrate, the first electrically insulating layer being at a bonding interface between the first donor substrate and the carrier substrate, and the first donor substrate is detached along the weakened zone in order to transfer the first electrically insulating layer and the first single-crystal semiconductor layer to the carrier substrate, so as to form a first semiconductor-on-insulator substrate, said first layer-transfer step comprising a heat treatment at a sufficiently high temperature to smooth the first single-crystal semiconductor layer that is transferred onto the carrier substrate to a roughness lower than 0.1 nm RMS,

- after said heat treatment, a second layer-transfer step comprising forming a weakened zone in a second donor substrate by implantation of atomic species, the second donor substrate is bonded to the first single-crystal semiconductor layer, the second electrically insulating layer being at a bonding interface between the second donor substrate and the first single-crystal semiconductor layer, and the second donor substrate is detached along the weakened zone in order to transfer the second electrically insulating layer and the second single-crystal semiconductor layer to the first single-crystal semiconductor layer of the first semiconductor-on-insulator substrate.

2. The process as claimed in claim 1, wherein the trenches are formed by etching, the first electrically insulating layer forming a stop layer for said etching.

3. The process as claimed in either one of claims 1 and 2, wherein the thickness of the first and second single-crystal semiconductor layers is comprised between 25 and 40 nm.

4. The process as claimed in one of claims 1 to 3, wherein the first and second semiconductor layers are made of silicon doped opposite types.

5. The process as claimed in one of claims 1 to 3, wherein the first and second semiconductor layers are made of silicon having different crystal orientations.

6. The process as claimed in one of claims 1 to 3, wherein the first and second semiconductor layers are made of different materials.

7. The device as claimed in one of claims 1 to 3 and 6, wherein the semiconductor layer in which the channel of an n-type transistor is formed is made of strained silicon.

8. The process as claimed in one of claims 1 to 3 and 6 and 7, wherein the semiconductor layer in which the channel of a p-type transistor is formed is made of silicon-germanium.

9. The process as claimed in one of claims 1 to 8, wherein the first and/or second electrically insulating layers are made of silicon oxide (SiO_2).

10. The process as claimed in one of claims 1 to 8, wherein the first and second electrically insulating layers are made of different materials.

11. The process as claimed in one of claims 1 to 8 and 10, wherein the first electrically insulating layer is made of a high-k material.

12. The process as claimed in one of claims 1 to 8, 10 and 11, wherein the second electrically insulating layer is made of a low-k material.

13. The process as claimed in one of claims 1 to 12, comprising growing by epitaxy a semiconductor layer on the carrier substrate.

14. The process as claimed in one of claims 1 to 12, wherein the carrier substrate comprises at least one COP-free CZ silicon layer.

15. The process as claimed in one of claims 1 to 13, wherein the smoothing heat treatment of the first single-crystal semiconductor layer is carried out at a temperature comprised between 1000 and 1200°C, for a time comprised between 10 and 120 minutes.

16. The process as claimed in one of claims 1 to 15, furthermore comprising a heat treatment for finishing the second single-crystal semiconductor layer at a temperature comprised between 1100 and 1250°C, carried out for a time shorter than one minute.