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(54) A DYNAMIC BISTABLE CIRCUIT

(71) We, TIMEX CORPORATION, a corporation organised under the laws of the State of Delaware, U.S.A., of Waterbury, Connecticut 06720, United States of America, do hereby declare the invention, for which we pray that a Patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention relates to a dynamic bistable circuit. The invention finds particular, but not exclusive, application in horological movements.

One of the basic types of circuits is a "divide-by-two" count-down circuit in which an input frequency is divided by a factor of two. Such circuits may be connected in series to form a multi-stage binary counter.

It has been suggested that the count-down divide-by-two circuit should be statically bistable. Such a bistable circuit is triggered into one state by a first pulse and holds that one state until triggered into its other state by a subsequent pulse. The pulses may be, for example, from a frequency source, such as a crystal oscillator, or from a preceding count-down circuit. Such circuits, which are able to hold either of their states indefinitely until triggered, require a relatively large number of transistors, for example, sixteen transistors in one stage, and consequently may be relatively complex to manufacture and relatively high in power consumption.

It has also been suggested that the count-down circuit be dynamic, that is, a count-down circuit which will not hold its state indefinitely. If the input frequency is sufficiently high, for example, above one KHz then the subsequent trigger pulse arrives before the circuit has, on its own, changed state. Such dynamic count-down circuits may require fewer transistors and have a lower power consumption than the statically stable types of circuits.

In accordance with the present invention there is provided a dynamic bistable circuit comprising a first gating circuit consisting of a first pair of complementary MOS field effect transistors, a second gating circuit consisting

of a second pair of complementary MOS field effect transistors, each of said transistors having a gate electrode, a source electrode and a drain electrode, and each transistor of said second pair of transistors has its gate electrode connected to a common connection of the drain electrodes of said first pair of transistors, each of the source electrodes of said first and second pair of transistors is connected to receive successive pulse signals, and wherein the pulse signals being successively applied at least to the source electrodes of said second pair of transistors are at a rate to define an input frequency for the dynamic circuit, and wherein the output signal is taken from the common connection of the drain electrodes of the second pair of transistors and a feedback circuit for converting the output signal into a feedback signal which controls said first pair of transistors.

In order to save space, reduce cost, and provide a low power consumption, the circuit of the present invention is preferably "integrated", that is, the entire circuit is formed on a single chip (usually flat wafer) of base material, such as silicon, although the circuit is "complementary", that is, its transistors are of the P-channel and N-channel types.

In some applications, and particularly in wrist watches, the power consumption of the binary counter circuitry may be of critical importance. In a quartz crystal watch the high frequency of a quartz crystal oscillator, which is the frequency standard, is divided down to produce time pulses which may be directly displayed for example, on an electro-optical liquid crystal display, or which may synchronize a motor which drives a time display, or which directly drives a motor which operates a time display.

A number of embodiments of the present invention will be described. However, each of those embodiments utilize a gating circuit, which is part of the circuit. The gating circuit is connected to a circuit, or generator, which changes the polarity of a D.C. voltage source. In a watch the D.C. source is a small battery cell within the watch case. The

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transistors are preferably Field Effect Transistors (FET) of the enhancement type.

In order that the invention may be better understood, several embodiments thereof will now be described by way of example only and with reference to the accompanying drawings in which:—

Figure 1 is a schematic diagram of a first embodiment of the present invention which operates as a flip-flop;

Figure 2 is a schematic diagram of a second embodiment of the present invention, which operates as a binary divider;

Figure 3 is a schematic diagram illustrating the basic gating circuit used in the bistable circuit of the invention; and

Figure 4 is a schematic diagram showing the use of the circuit of Figure 1 in an electronic watch.

The first embodiment of the present invention, shown in Figure 1 is a divide-by-two count-down integrated circuit. In an integrated circuit all the components and interconnections are fabricated by processing appropriate areas of a single crystal semi-conductive wafer (chip) such as a silicon wafer. The entire wafer is kept to a micro-miniature size. Generally, each of the wafers may consist of silicon which provides the substrate onto which various components are produced by diffusion. Alternatively, other methods of forming the integrated circuit may be used, such as ion implantation or layer deposition.

The transistors are metal oxide semi-conductor field effect transistors, hereinafter referred to as MOSFET's. As illustrated in the accompanying drawings, the MOSFET's are either N-channel and P-channel enhancement mode. In the N-channel enhancement transistors the arrow is pointing toward the channel (toward the device). The enhancement type of MOSFET is non-conducting ("off" or "not enabled") until voltage of the correct polarity is applied to the gate electrode. In the case of an N-channel device, such as transistor 11 of Figure 1, a positive voltage applied to the gate electrode (which varies the impedance of the device), over input lead 13, will change the channel region beneath the gate to thereby provide a conduction path between its N-type source and its N-type drain electrodes (called the high impedance electrodes). Conversely, in the P-channel transistor, such as transistor 10, a negative voltage on line 12 is required for conduction.

The circuit of Figure 1 functions as a "flip-flop", that is, it has two stable states and is switched from one state to the other by a reversal of polarity. The circuit produces an

output voltage level for each complete cycle, so that it produces one output pulse for every two input pulses.

The circuit consists of eight MOS transistors in an integrated circuit. The eight transistors are arranged in four pairs, each pair using a gating circuit of the basic form shown in Figure 3. Each gating circuit comprises a pair of complementary MOS transistors interconnected as shown. It is assumed that the absence of a pulse, i.e., earth voltage level, is a logic "0" and the presence of a positive pulse is a logic "1". The original polarity at the input leads 12 and 13 is respectively positive and negative and 180° out of phase.

Pulse signals each comprising successive reversals of polarity are applied to respective leads 12 and 13, such reversals of polarity defining the incoming frequency. When a reversal of polarity occurs, a negative (−) voltage pulse appears on lead 12 and a positive (+) voltage on lead 13, and, upon the next reversal, a positive voltage pulse appears on lead 12 and a negative voltage pulse on lead 13. The reversals of polarity are obtained from a polarity reversal circuit (not shown) which may use a flip-flop and other circuitry.

In operation, after the circuit has commenced operation, during the "first period", as shown in Table 1 below, there exists a "0" level at point D, a negative polarity on lead 13 and a positive polarity on lead 12, and the circuit is in one of its stable states. In the "second period" the polarity is reversed, and a negative voltage is applied to lead 12 and a positive voltage to lead 13. The "0" level from point D is applied to point A through lead 14, transistor 11 and lead 15. The polarity is again reversed in the "third period", i.e. positive voltage is on lead 12 and negative voltage on lead 13. The voltage at point A (its distributed parasitic capacitance) enables the gate 16a of transistor 16. Consequently, the level at point B becomes "1", the level at point C becomes "0" (because the gate of transistor 19 is also enabled), and the level at point D becomes "1" (because the gate of transistor 20 is enabled). In the "fourth period" the polarity is again reversed, with negative voltage on line 12, and point A becomes a "1" level, point B at a "1" level, point C at "0", and point D at a "1" level. The following period is a repetition of Period 1 and so forth.

These relationships are illustrated in the following Table. The operation of the circuit is based upon retaining (trapping) the voltage at point A by the distributed parasitic capacitance at that point.

TABLE 1

Period	A	B	C	D	Transistor 11	Transistor 17	lead 13	output
1	1	0	1	0	off	on	—	0
2	0	0	1	0	on	off	+	0
3	0	1	0	1	off	off	—	1
4	1	1	0	1	off	off	+	1

One will note that points B and D are at the same logic state, for example, both are at a "0" level at the same time. Consequently, B and D may be connected together and the transistors 18, 19, 20 and 21 eliminated. However, the remaining transistors 10, 11, 16 and 17 would have to be balanced, which may add additional time and cost to the manufacturing process. As shown in the chart above, the output 22 changes state once during the four periods and the lead 13 (and lead 12) has four different polarities, which provides the divide-by-two result. It will also be seen that the pulse levels at points C, D, are inverted with respect to the pulse levels at the points B, C, respectively.

A binary divider is shown in Figure 2 as another embodiment of the present invention utilizing a bistable dynamic circuit. The circuit of Figure 2 utilizes three complementary pairs of MOSFET transistors, each pair uses a gating circuit of the basic type shown in Figure 3. In this embodiment the pulsed power supplies having reversals of polarities are applied to the leads 40, 41, 42 and 43, which are sources of the transistors 44, 45, 46 and 47. The polarities of leads 41 and 42 are the same, and consequently those leads may also be connected together. The polarity of the pulses applied to the first gating circuit, which consists of transistors 44 and 45, is opposite to the polarity of the second gating circuit, consisting of transistors 46 and 47. For example, a positive pulse may be applied to lead 40 simultaneously with the negative pulse being applied to the lead 42. The opposite polarity would be applied simultaneously to the leads 41 and 43, namely, negative to lead 41 and positive to lead 43.

The operation of the circuit of Figure 2 is set forth in Table 2 below, which covers four periods and looks at the circuit during its operation. It will be noted that, during those four periods there are, for example, on lead 40, two input pulses. At the output lead 51 these occurs, however, only two changes of state. Consequently, for the four input states on the lead 40 there are two output states at the output 51. The operation of Figure 2 assumes a "0" level at point C, which is between the transistors 49 and 50 when there is a negative voltage on lead 40. That "0" level, causes a "1" level at point A when lead 40 becomes positive. When lead 40 again becomes negative, the voltage at

point A, stored by the parasitic capacitance, enables the gate of transistor 47, causing point B to revert to a "0" level and point C by inversion to a "1" level. The next reversal of polarity causes A to revert to an "0" level, which is stored at A when lead 40 again goes to negative. Simultaneously the point B reverts to a "1" level and point C by inversion to a "0" level.

TABLE 2

Period	A	B	C	lead 40	output
1	0	1	0	—	0
2	1	1	0	+	0
3	1	0	1	—	1
4	0	0	1	+	1
5	0	1	0	—	0

As shown in Figure 4, the apparatus of the present invention may be used in a watch case, and a crystal controlled oscillator, preferably with a frequency of 32,768 Hz, which is connected to, for example, a pulse generator circuit 82. The dynamic divider 83 is a series of multi-stage divide-by-two circuits of the type shown in Figure 1. It is connected to a conventional static multi-stage divide-by-two circuit 86. The display driver 84 may be an electromechanical converting motor to drive the hands of the display 85, or a circuit to convert the frequency into digital numerical form to show on an electro-optical display 85.

It will be understood that the terms "drain" and "source" as used herein, refer to the connections of the MOSFET devices and not to their structure, as generally their structure is symmetric and the drain and source connection may be interchanged.

WHAT WE CLAIM IS:—

1. A dynamic bistable circuit comprising a first gating circuit consisting of a first pair of complementary MOS field effect transistors, a second gating circuit consisting of a second pair of complementary MOS field effect transistors, each of said transistors having a gate electrode, a source electrode and a drain electrode, and each transistor of said second pair of transistors has its gate electrode connected to a common connection of the drain electrodes of said first pair of transistors, each of the source electrodes of said first and second pair of transistors is connected to receive successive pulse signals, and wherein the

TABLE 1

Period	A	B	C	D	Transistor 11	Transistor 17	lead 13	output
1	1	0	1	0	off	on	-	0
2	0	0	1	0	on	off	+	0
3	0	1	0	1	off	off	-	1
4	1	1	0	1	off	off	+	1

One will note that points B and D are at the same logic state, for example, both are at a "0" level at the same time. Consequently, B and D may be connected together and the transistors 18, 19, 20 and 21 eliminated. However, the remaining transistors 10, 11, 16 and 17 would have to be balanced, which may add additional time and cost to the manufacturing process. As shown in the chart above, the output 22 changes state once during the four periods and the lead 13 (and lead 12) has four different polarities, which provides the divide-by-two result. It will also be seen that the pulse levels at points C, D, are inverted with respect to the pulse levels at the points B, C, respectively.

A binary divider is shown in Figure 2 as another embodiment of the present invention utilizing a bistable dynamic circuit. The circuit of Figure 2 utilizes three complementary pairs of MOSFET transistors, each pair uses a gating circuit of the basic type shown in Figure 3. In this embodiment the pulsed power supplies having reversals of polarities are applied to the leads 40, 41, 42 and 43, which are sources of the transistors 44, 45, 46 and 47. The polarities of leads 41 and 42 are the same, and consequently those leads may also be connected together. The polarity of the pulses applied to the first gating circuit, which consists of transistors 44 and 45, is opposite to the polarity of the second gating circuit, consisting of transistors 46 and 47. For example, a positive pulse may be applied to lead 40 simultaneously with the negative pulse being applied to the lead 42. The opposite polarity would be applied simultaneously to the leads 41 and 43, namely, negative to lead 41 and positive to lead 43.

The operation of the circuit of Figure 2 is set forth in Table 2 below, which covers four periods and looks at the circuit during its operation. It will be noted that, during those four periods there are, for example, on lead 40, two input pulses. At the output lead 51 these occurs, however, only two changes of state. Consequently, for the four input states on the lead 40 there are two output states at the output 51. The operation of Figure 2 assumes a "0" level at point C, which is between the transistors 49 and 50 when there is a negative voltage on lead 40. That "0" level, causes a "1" level at point A when lead 40 becomes positive. When lead 40 again becomes negative, the voltage at

point A, stored by the parasitic capacitance, enables the gate of transistor 47, causing point B to revert to a "0" level and point C by inversion to a "1" level. The next reversal of polarity causes A to revert to an "0" level, which is stored at A when lead 40 again goes to negative. Simultaneously the point B reverts to a "1" level and point C by inversion to a "0" level.

Period	A	B	C	lead 40	output
1	0	1	0	-	0
2	1	1	0	+	0
3	1	0	1	-	1
4	0	0	1	+	1
5	0	1	0	-	0

As shown in Figure 4, the apparatus of the present invention may be used in a watch case, and a crystal controlled oscillator, preferably with a frequency of 32,768 Hz, which is connected to, for example, a pulse generator circuit 82. The dynamic divider 83 is a series of multi-stage divide-by-two circuits of the type shown in Figure 1. It is connected to a conventional static multi-stage divide-by-two circuit 86. The display driver 84 may be an electromechanical converting motor to drive the hands of the display 85, or a circuit to convert the frequency into digital numerical form to show on an electro-optical display 85.

It will be understood that the terms "drain" and "source" as used herein, refer to the connections of the MOSFET devices and not to their structure, as generally their structure is symmetric and the drain and source connection may be interchanged.

WHAT WE CLAIM IS:—

1. A dynamic bistable circuit comprising a first gating circuit consisting of a first pair of complementary MOS field effect transistors, a second gating circuit consisting of a second pair of complementary MOS field effect transistors, each of said transistors having a gate electrode, a source electrode and a drain electrode, and each transistor of said second pair of transistors has its gate electrode connected to a common connection of the drain electrodes of said first pair of transistors, each of the source electrodes of said first and second pair of transistors is connected to receive successive pulse signals, and wherein the



pulse signals being successively applied at least to the source electrodes of said second pair of transistors are at a rate to define an input frequency for the dynamic circuit, and wherein the output signal is taken from the common connection of the drain electrodes of the second pair of transistors, and a feedback circuit for converting the output signal into a feedback signal which controls said first pair of transistors.

2. A dynamic bistable circuit as claimed in claim 1 wherein the gate electrode of each of the first pair of transistors is connected to the source electrode of a respective transistor of the second pair and wherein the feedback signal is passed to the common connection of the source electrodes of the first pair of transistors, the feedback signal thus constituting the pulse signal received by the source electrodes of the first pair of transistors.

3. A dynamic circuit as claimed in claim 2 wherein the feedback circuit comprises a first and a second inverter circuit consisting respectively of a third and a fourth pair of complementary MOS field effect transistors, each of said transistors having a control gate electrode, a source electrode and a drain electrode, and wherein each transistor of said third pair of transistors has its gate electrode connected to the common connection of the drain electrodes of said second pair of transistors, each transistor of said fourth pair of transistors has its gate electrode connected to a common connection of the drain electrodes of said third pair of transistors; and wherein the feedback signal is taken from the common connection of the drain electrodes of said fourth pair of transistors, which latter common connection constitutes the output of the circuit.

4. A dynamic bistable circuit as claimed in claim 1 wherein the source electrode of each of the first pair of transistors is connected to the source electrode of a transistor of the second pair, and wherein the feedback signal is passed to the common connection of the gate electrodes of the first pair of transistors.

5. A dynamic circuit as claimed in claim 4 wherein the feedback circuit comprises a first inverter circuit consisting of a third pair of complementary MOS field effect transistors, each of said transistors having a gate electrode, a drain electrode, and a source electrode; and wherein the gate electrodes of said third pair of transistors are both connected to the common connection of the drain electrodes of said second pair of transistors; the feedback signal being taken from the common connection of the drain electrodes of said third pair of transistors which latter common connection constitutes the output of the circuit.

6. A dynamic circuit as claimed in any one of the preceding claims further including a pulse generator circuit for providing said pulse signals.

7. A dynamic bistable circuit substantially as herein before described with reference to the accompanying drawings.

8. A dynamic bistable circuit as claimed in any one of the preceding claims made in the form of an integrated circuit.

9. A counter consisting of a series of dynamic bistable circuits as claimed in any one of the preceding claims.

10. A horological movement including an electrical power source, an oscillator connected to said power source, a dynamic bistable circuit as claimed in any one of claims 1 to 8, a pulse generator circuit for generating said pulse signals, the input of said pulse generator circuit being connected to said oscillator, a static bistable divider whose input is connected to said dynamic circuit, a display drive whose input is connected to said static divider, and a display whose input is connected to said display driver.

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