Claims

1. A 3D semiconductor device, the device comprising:

a first die, comprising a first die area and a plurality of first die top contacts;

a second die, comprising a second die area and a plurality of first bottom contacts; and

a third die, comprising a third die area and a plurality of second bottom contacts,

wherein said first die area is greater than the sum of said second die area and said third die area,

wherein said second die and said third die are both placed on top of said first die laterally with respect to each other,

wherein said plurality of first bottom contacts are connected to said first die top contacts, and

wherein said plurality of second bottom contacts are connected to said first die top contacts.

2. The device according to claim 1,

wherein said first die comprises a plurality of third bottom contacts, and

wherein said third bottom contacts are adapted to provide connection to an external device.

3. The device according to claim 1,

wherein said second die is processed by a different fab process line than said third die.

4. The device according to claim 1,

wherein said second die is primarily a memory device and said third die is primarily a logic device.

5. The device according to claim 1,

wherein said first die is an electrically configurable device.

6. The device according to claim 1,

wherein said second die is primarily an Input/Output device.

7. The device according to claim 1,

wherein said second die is primarily an FPGA device.

8. A 3D semiconductor device, the device comprising:

a first die, comprising a first die area and a plurality of first die top contacts;

a second die, comprising a second die area and a plurality of first bottom contacts;

a third die, comprising a third die area and a plurality of second bottom contacts; and

a fourth die, comprising a fourth die area and a plurality of third bottom contacts,

wherein said first die area is greater than the sum of said second die area, said third die area, and said fourth die area,

wherein said second die, said third die, and said fourth die are all placed on top of said first die laterally with respect to each other,

wherein said plurality of first bottom contacts are connected to said first die top contacts,

wherein said plurality of second bottom contacts are connected to said first die top contacts, and

wherein said plurality of third bottom contacts are connected to said first die top contacts.

9. The device according to claim 8,

wherein said first die comprises a plurality of fourth bottom contacts, and

wherein said fourth bottom contacts are adapted to provide connection to an external device.

10. The device according to claim 8,

wherein said second die is processed by a different fab process line than said third die.

11. The device according to claim 8,

wherein said second die is primarily a memory device and said third die is primarily a logic device.

12. The device according to claim 8,

wherein said first die is an electrically configurable device.

13. The device according to claim 8,

wherein said second die is primarily an Input/Output device.

14. The device according to claim 8,

wherein said second die is primarily an FPGA device.

15. A 3D semiconductor device, the device comprising:

a first die, comprising a first die area and a plurality of first die top contacts;

a second die, comprising a second die area and a plurality of first bottom contacts; and

a third die, comprising a third die area and a plurality of second bottom contacts,

wherein said first die area is greater than second die area,

wherein said second die and said third die are both placed on top of said first die laterally with respect to each other,

wherein said plurality of first bottom contacts are connected to said first die top contacts,

wherein said second die comprises a plurality of second top contacts,

wherein said plurality of second bottom contacts are connected to said plurality of second top contacts.

16. The device according to claim 15,

wherein said first die comprises a plurality of third bottom contacts, and

wherein said third bottom contacts are adapted to provide connection to an external device.

17. The device according to claim 15,

wherein said second die is processed by a different fab process line than said third die.

18. The device according to claim 15,

wherein said first die is an electrically configurable device.

19. The device according to claim 15,

wherein said third die is primarily an Input/Output device.

20. The device according to claim 15,

wherein said second die is primarily an FPGA device.