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IMAGE PROCESSING APPARATUS AND METHOD

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to an apparatus and method for encoding an image. More particularly, it pertains to an apparatus and method for quantizing conversion data obtained by transforming image information to a frequency space so as to encode such data.

Related Background Art

An Adaptive Discrete Cosine Transformation (ADCT) encoding system used as a method for encoding color image signals has gained attention in recent years. A Joint Photographic Expert Group (JPEG), which was founded as an international organization for standardizing such an encoding system, will soon adapt the ADCT encoding system as an official encoding system.

The outline of such an encoding system will be described briefly.

Fig. 3 is a block diagram illustrating the approximate structure of a conventional encoding system utilizing DCT. Figs. 4A to 4D are views illustrating the encoding system shown in Fig. 3. Numeral 2 denotes an input terminal of a digital image signal to be encoded. A raster scanned digital image signal is input from a CCD

sensor (not shown) to the input terminal 2, and then to an 8 x 8 block formation circuit 4, where it is second dimensionally divided into 8 x 8 pixel blocks, and then transmitted pixel block by pixel block to components connected to the formation circuit 4.

Numeral 6 denotes a DCT converting circuit for changing the image signal transmitted from the block formation circuit 4 into discrete cosine transformation so as to output 8 x 8 data matrixes regarding a frequency zone. In other words, the DCT converting circuit 6 converts pixel blocks forming image data items D_{11} to D_{88} shown in Fig. 4A into data matrixes forming DCT coefficients X_{11} to X_{88} shown in Fig. 4B.

Data matrix X_{11} represents a DC component in horizontal and vertical directions of the pixel block, that is, the average value of the pixel block. When the DCT coefficients X_{11} to X_{88} are expressed as Xij, the greater the "i" increases, the higher the frequency a component has in the vertical direction; similarly, the greater the "j" increases, the higher the frequency the component has in the horizontal direction.

The data matrixes output from the DCT converting circuit 6 are input to a linear quantization circuit 8. A quantization matrix generation circuit 18 generates quantization matrixes W_{11} to W_{88} (shown in Fig. 4C) which

show the weight of a step of quantizing the DCT coefficients X_{11} to X_{88}. A coefficient generation circuit 16 generates coefficients C. The quantization matrixes W_{11} to W_{88} and the coefficients C are input to a multiplier 20. The multiplier 20 calculates an equation $(W_{ij} \times C/C_0)$. A quantizing step performed by the linear quantization circuit 8 is determined in accordance with the outputs Q_{11} to Q_{88} of the multiplier 20. The coefficients C are positive values which control image quality and the amount of data generated, whereas C_0 is a constant.

The linear quantization circuit 8 actually calculates an equation X_{ij}/Q_{ij}, and outputs it. The outputs of the linear quantization circuit 8 are expressed as quantized conversion data items G_{11} to G_{88}. The quantized data items G_{11} to G_{88} are successively transmitted starting from DC-components from a zigzag scan circuit 10. In other words, the data items G_{11} to G_{88} are supplied from the zigzag circuit 10 to a Variable Length Coding (VLC) circuit 12 in the order of G_{11}, G_{12}, G_{21}, G_{31}, G_{22}, G_{13}, G_{14}, G_{23}, G_{32}, G_{41} $\cdots$ G_{85}, G_{86}, G_{77}, G_{68}, G_{78} and G_{88}.

As regards, for example, a DC component G_{11}, the VLC circuit 12 calculates a predicted value between pixel blocks located near the DC component G_{11}, and changes a difference between the predicted value and an actual value into a Huffman code. As regards AC components G_{12} to G_{88},

since most of the coefficients appear to be zeros, group ID numbers, which identify groups into which significant coefficients except zero are divided according to the values of the significant coefficients, and values combined with the number of zeros preceded by the significant coefficients (run length of zeros) are formed into Huffman codes by the VLC circuit 12. Data indicating values in the groups, into which the significant coefficients are divided, is additionally coded.

In general, since the ratio at which high-frequency components occur in the diagonal direction of an image is low, it is predicted that, after zigzag scanning has been performed, in many cases all components become zero which occupy the latter half of the outputs represented by Gij and transmitted from the line quantization circuit 8. It is therefore expected that variable length codes thus obtained can be compressed at a very high ratio. If a compression ratio between 1 out of 2 and 1 out of 9 is employed, it is possible to reproduce an image having hardly deteriorated quality.

Generally, the amount of data transmitted through a transmission route per unit time is fixed. When one screen must be transmitted at each predetermined time interval, as when an image is transmitted, it is desirable that an output code be represented by a bit number fixed by an

image or pixel block unit.

If a high value is given to the coefficients C mentioned previously, the ratio at which Gij assumes zero increases and the total number of bits of encoded data NB decreases. The relationship between the coefficients C and the total number of bits NB varies according to images, and is expressed by a monotone decreasing function. It is known that such a relationship regarding an average image is expressed by the logarithmic curve shown in Fig. 4D.

The above-mentioned JPEG presents a method of predicting a coefficient C_0 for obtaining the desired total number of bits NB0. A coefficient C_1 is first encoded, and then the total number of bits nb1 of a thus-obtained code is determined. A predicted value C_2 of the coefficient C_0 is calculated on the basis of the total number of bits nb1. Such calculation can be predicted because the logarithmic curve shown in Fig. 4D runs through a point (C_1, nb1).

By repeating the above operation several times, the amount of data encoded can be obtained within approximately several % errors with respect to the desired total number of bits NB0.

However, the process of repeatedly encoding data so as to determine the coefficients C is a very time-consuming process, and is not suitable for an encoding apparatus which is required to transmit one screen at predetermined

time intervals, such as moving images. Such a process is extremely difficult to perform in terms of calculation speed, particularly when image signals of a very high bit rate, such as high definition television signals, are handled.

SUMMARY OF THE INVENTION

The present invention has been made in view of the above problems, and an object thereof is to provide a simply-constructed image processing apparatus suitable for obtaining a predetermined amount of encoded data.

To achieve the above object, in accordance with one aspect of this invention, an image processing apparatus comprises input means for inputting image data; quantizing means for quantizing the image data and outputting quantized digital data; first encoding means for encoding the quantized digital data and outputting first encoded data; second encoding means for encoding data a bit sifted from the quantized digital data and second encoded data; and calculating means for calculating a suitable quantizing parameter for quantizing the image data in accordance with the first and second encoded data.

Another object of this invention is to provide an encoding method suitable for encoding moving images.

A further object is to provide a high-speed encoding method.

The embodiments and other objects of this invention will become apparent from the description and claim taken in connection with the following drawing.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a view showing a first embodiment of the present invention;

Fig. 2 is a view showing a second embodiment of this invention;

Fig. 3 is a view showing the conventional art; and

Figs. 4A to 4D are views illustrating the encoding method shown in Fig. 3.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

According to the embodiments of the present invention which will be described below, an encoding apparatus, which quantizes data obtained by transforming image information to a frequency zone and then forms such data into variable length codes, comprises a plurality of quantizing, a calculating, a calculating and generating, and a selecting means. The quantizing means perform control on the basis of a first set of control coefficients; the calculating means calculates the amount of data when a plurality of quantized data are formed into variable length codes; the calculating and generating means calculates and generates a second set of control coefficients; and the selecting means selects outputs which are quantized and formed into

variable length codes using the second set of control coefficients.

Because of the structure as described above, the control coefficients obtained by a second quantizing means approach desired values as compared with a first quantizing means. Control coefficients substantially close to the desired control coefficients can be obtained. Since it is not necessary to repeatedly encode data and calculate the control coefficients, a process can be performed at extremely high speed. The apparatus can be thoroughly applied to processing moving images.

The embodiments of this invention will be described below in detail. Fig. 1 is a block diagram showing the first embodiment of this invention.

In this figure, numeral 20 denotes an input terminal of an analog television signal. A television signal input through the terminal 20 is digitized by an A/D convertor 22 into 8-bit data. The 8-bit data is then divided by an 8 x 8 block formation circuit 26 into 8 x 8 pixel blocks, and supplied to a DCT converting circuit 28 block by block. The 8 x 8 block formation circuit 26 operates in the same manner as the block formation circuit 4 shown in Fig. 3.

As in Fig. 3, pixel data items D_{11} to D_{88} in blocks are converted by the DCT converting circuit 28 into data matrixes X_{11} to X_{88} regarding the frequency zones, and are

supplied to a zigzag scan circuit 30. The zigzag scan circuit 30 operates in the same manner as the zigzag scan circuit 10 shown in Fig. 3, and outputs the DCT converted data matrixes X_{11} to X_{88} in the order of X_{11}, X_{12}, X_{21}, X_{31}, X_{22}, X_{13}, X_{14}, X_{23}, X_{32}, X_{41} $\cdots$ X_{85}, X_{86}, X_{77}, X_{68}, X_{78}, X_{87} and X_{88}.

A quantization matrix generation circuit 36 generates the quantized matrixes X_{11} to X_{88}. However, in this embodiment, since data which has already been quantized is input to quantization circuits 32a to 32d, the quantized matrixes X_{11} to X_{88} are generated in an order corresponding to the order of zigzag scanning, and supplied to multipliers 38a to 38d.

Initial coefficients C_1 to C_4, serving as control coefficients C, are fed from a coefficient calculator 48 to the multipliers 38a to 38d, respectively. In the same manner as in the conventional art described previously, the multipliers 38a to 38d calculate the quantized matrixes X_{11} to X_{88} and the control coefficients C_x using an equation $(W_{ij} \times C_x/C_0)$, and output them to the quantization circuits 32a to 32d. The quantization circuits 32a to 32d quantize conversion coefficients, which are controlled by the control coefficients C_1 to C_4, and zigzag-scanned in a quantizing step. The quantization circuits 32a to 32d output these coefficients to variable length coders (VLCs)

40a to 40d.

In this embodiment, the VLCs 40a to 40d do not output data which has actually been encoded, but only output information nb1 to nb4 regarding the total number of bits of each screen when the VLCs 40a to 40d perform the same process as the VLC 12 shown in Fig. 3.

The coefficient calculator 48 calculates a control coefficient C_5 used for the desired total number of bits and outputs it to a multiplier 38e. This calculation is performed using the control coefficients C_1 to C_4 and the information nb1 to nb4 output from the VLCs 40a to 40d, respectively.

The coefficient calculator 48 outputs control coefficients C_6 and C_7, which are values approximate to the control coefficient C_5, to multipliers 38f and 38g and to terminals 44a to 44c of a switch 44.

However, when C_5 is greater than or equal to C_n and less than or equal to C_{n+1} ($C_n \leq C_5 \leq C_{n+1}$), then C_6 is greater than or equal to C_n and less than C_5 ($C_n \leq C_6 < C_5$), and C_7 is greater than C_5 and less than or equal to C_{n+1} ($C_5 < C_7 \leq C_{n+1}$), where n is greater than or equal to 1 and less than or equal to 3 ($1 \leq n \leq 3$).

The matrixes and the coefficients are calculated by the quantization matrix generation circuit 36 and using the control coefficients C_5 to C_7. In the same way as the above-mentioned multipliers 38a to 38d, the multipliers 38e

to 38g output the matrixes and the control coefficients to quantization circuits 32e to 32g during a vertical blanking period.

A DCT conversion coefficient is output from the zigzag scan circuit 30, delayed by a one-frame delay circuit 34, and then input to quantization circuits 32e to 32g.

The quantization circuits 32e to 32g quantize the conversion coefficient, which has been controlled by the control coefficients C_5 and C_6 in a quantizing step, and output it to variable length coders (VLCs) 40e to 40g. In this embodiment, the VLCs 40e to 40g not only output data which has actually been encoded to entry buffers 42a to 42c, but also output the total number of bits nb5 to nb7 to a judgment circuit 50. The judgment circuit 50 outputs, to switches 44 and 46, data which selects the result of quantizing the conversion coefficient so that the result is nearest but not more than the desired total number of bits. The entry buffers 42a to 42c accumulate encoded data until the judgement circuit 50 outputs the result of judgement. The switch 44 selects the control coefficients on the basis of the judgement, and outputs them to a multiplexer 52. The switch 46 selects the encoded data, and outputs it to the multiplexer 52. The multiplexer 52 multiplexes the control coefficients and encoded data, and outputs them to an output terminal 54.

Fig. 2 is a block diagram showing the second embodiment of this invention. Components operating in the same manner as those in the first embodiment are identified by the same reference characters.

A DCT coefficient from a zigzag circuit 30 is output to a one-frame delay circuit 34 and a quantization circuit 60. A multiplier 62 first calculates an initial coefficient C_1 and quantized matrixes W_{11} to W_{38} output from a quantization matrix generation circuit 36. The multiplier 62 then outputs the coefficient and quantized matrixes to the quantization circuit 60. The initial control coefficient C_1 is output from a coefficient calculator 64. The quantization circuit 60 quantizes the DCT coefficient which has been controlled by the control coefficient C_1, and outputs it to variable length coders (VLCs) 40a to 40d, this quantization being performed in a quantizing step. If the total number of bits of the quantized DCT coefficient is K bits, K bits are output to the VLC 40a; (K-1) bits are output to the low-order bit of the VLC 40b; (K-2) bits are output to the low-order bit of the VLC 40c; and (K-3) bits are output to the low-order bit of the VLC 40d. As in the first embodiment, the VLCs 40a to 40d do not output encoded data, but output to the coefficient calculator 64 only information nb1 to nb4

regarding the total number of bits of each screen. The output of the quantization circuit 60 is shifted 0 to 3 bits toward a low-order direction, and then connected. By such an operation, the VLC 40a changes a quantized output, which is controlled by the initial control coefficient C_1, into a variable length code; the VLC 40b changes a quantized output, which is quantized using a step size twice that of the initial control coefficient C_1, into a variable length code; the VLC 40c changes a quantized output, which is quantized using a step size four times that of the initial control coefficient C_1, into a variable length code; the VLC 40d changes a quantized output, which is quantized using a step size eight times that of the initial control coefficient C_1, into a variable length code. In other words, the amount of data, nb1 to nb4, formed into variable length codes represents the amount of data encoded by control coefficients C_1, $C_1 \times 2$, $C_1 \times 4$ and $C_1 \times 8$. It is thus possible to decrease the number of encoders and to simplify the structure of circuitry by shifting bits.

The coefficient calculator 64 determines a control coefficient C_5 with respect to the desired amount of encoding. This determination is based upon the amount of data, nb1 to nb4, formed into the variable length codes corresponding to the control coefficients C_1, $C_1 \times 2$, $C_1 \times$

4, and $C_1 \times 8$. The coefficient calculator 64 also determines not only $C_6 = C_5 - \alpha$, serving as a value approximate to the control coefficient C_5, but also $C_7 = C_5 + \alpha$, serving as a value approximate to the control coefficients C_6 and C_7. It outputs the control coefficients C_5 to C_7 to multipliers 38e to 38g, respectively. A process thereafter is performed in the same manner as in the first embodiment.

As has been described above, the image encoder of this invention, which quantizes data obtained by transforming image information to a frequency zone so as to form such data into variable length codes, is capable of setting the amount of data at every predetermined time interval to the desired amount and processing the data at very high speed.

The present invention may be applied to processing images in motion as well as at rest.

Bits may be shifted one by one or two by two.

Instead of controlling control coefficients, the contents of a quantization table may be changed.

The present invention is not limited to the embodiments described above, and various modifications and application may be possible within the scope of the claim.

This Sheet Has Been Replaced

C L A I M S H E E T

1. An image processing apparatus comprising:
input means for inputting digital image data;
extracting means for extracting upper part of the digital data; and
measuring means for measuring a data amount which is obtained when the upper part of the digital data is encoded.

2. An apparatus according to Claim 1, further comprising means for performing orthogonal transform on the image data.

3. An apparatus according to Claim 1, further comprising calculating means for calculating a suitable quantizing parameter for quantizing the digital image data.

4. An apparatus according to Claim 1, wherein the suitable parameter is a parameter which is set so that the amount of encoded image data of one screen is less than a predetermined amount.

5. An apparatus according to Claim 1, further comprising delaying means for delaying the image data while said measuring means performs measuring.

6. An apparatus according to Claim 1, wherein said apparatus is an apparatus for encoding moving images.

7. An image processing method comprising:
an input step of inputting digital image data;
an extracting step of extracting upper part of the quantized digital data; and
a measuring step of measuring a data amount which is obtained when the upper part of the quantized digital data is encoded.

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