

Abstract of the Disclosure

A data demodulator wholly consisting of digital circuits for TDMA signals subjected to differential phase-shift-keying (DPSK). The data demodulator generates a phase difference signal by subjecting $\pi/4$ QPSK signals to
5 delayed detection with phase detection means, delay means and phase difference detection means, connected in cascade and all known to persons skilled in the art, in synchronism with N-phase clock signals, and reproduces this phase difference signal into decision data with definition means.
10 A first such data demodulator finds out decision errors from said phase difference signal and decision data, and achieves symbol synchronism by sampling said decision data in a clock signal phase involving little decision error. A second such data demodulator supplies
15 said phase difference signal to said decision after correcting its D.C. offset due to a frequency drift. In these two data demodulators, the formulas for computing said decision errors and correction values are flexibly varied according to preceding burst information.

This Sheet Has Been Replaced

