CLAIMS

1. A microelectronic structure comprising:

a substrate (10) including an aperture (24) that penetrates through the substrate;

a conductor barrier layer (18) formed in, and partially filling, the aperture;

an annular conductor layer (20) formed on the microelectronic structure after forming of the barrier layer, the annular conductor layer being located at a periphery of the aperture and partially filling the aperture;

a conformal stop layer (22) formed over the annular conductive layer and partially filling the aperture;

a plug layer located surrounded by the conformal stop layer and filling the aperture, the plug layer comprising dielectric material; and

a base conductor layer in contact with the annular conductor layer

2. The microelectronic structure of claim 1 wherein the base conductor layer is in contact with a base portion of the conformal stop layer.

3. The microelectronic structure of claim 1 or claim 2 wherein the substrate comprises a ceramic substrate.

4. The microelectronic structure of claim 1 or claim 2 wherein the substrate comprises a semiconductor substrate.

5. The microelectronic structure of claim 1 or claim 2 wherein the annular conductor layer comprises a material selected from the group consisting of aluminum, copper, titanium, tantalum and tungsten.

6. The microelectronic structure of claim 1 or claim 2 further comprising an annular stop layer separating the plug layer from the annular conductor layer.

7. The microelectronic structure of claim 1 or claim 2 further comprising a conductor layer located above the substrate and contacting the annular conductor layer.

8. A semiconductor structure comprising:

a semiconductor substrate including an aperture that penetrates through the semiconductor substrate;

an annular barrier layer (18) formed in, and partially filling, the aperture;

an annular conductor layer (20) located upon the annular barrier layer and partially filling the aperture;

a planarization stop layer (22) located on sidewalls of the annular conductor layer and partially filling the aperture;

a plug layer located upon the planarization stop layer and filling the aperture; and

a base conductor layer formed on a planarized bottom surface of the semiconductor substrate, the base conductor layer in contact with the ~~conductor~~ annular barrier layer and the annular conductor layer.

9. The semiconductor structure of claim 8 wherein the base conductor layer is in contact with the base portion of the conformal stop layer.

10. A method for fabricating a microelectronic structure comprising:

an aperture forming step of forming a blind aperture within a substrate (10);

a layer-forming step of forming within the blind aperture a conformal conductor layer (20) that does not completely fill the blind aperture and a plug layer (24) that does completely fill the aperture; and

planarizing a backside of the substrate (10) to expose at least the conformal conductor layer (20); characterised by

the layer-forming step comprising successive layering and subsequently planarizing the conductor layer (20) and the plug layer (24), and further comprising forming a conformal stop layer (22) on a base and sidewalls of the conformal conductor layer (20) and by

forming a conductor layer under the substrate and contacting the planarized conformal conductor layer.

11. The method of claim 10 wherein the forming the blind aperture provides the blind aperture with a linewidth from about 5 to about 15 microns and an aspect ratio from about 1:10 to about 1:30.

12. The method of claim 10 wherein the successive layering further comprises successive layering a conformal liner layer into the aperture prior to the successive layering of the conformal conductor layer.

13. The method of claim 10 wherein the successive layering further comprises successive layering a conformal stop layer after successive layering the conformal conductor layer and prior to successive layering the plug layer.

14. The method of claim 10 wherein the planarizing the backside exposes the conformal conductor layer and the plug layer.

15. The method of claim 10 further comprising forming a conductor layer over the substrate and contacting a planarized conformal conductor layer.

16. The method of claim 10 further comprising forming a conductor layer under the substrate and contacting the planarized conformal conductor layer.

17. A method for fabricating a microelectronic structure comprising:

forming a blind aperture within a semiconductor substrate;

forming within the blind aperture a conformal dielectric liner layer (17) that partially fills the aperture, a conformal conductor layer (20) that partially fills the blind aperture, a conformal planarization stop layer (22) that partially fills the aperture and a plug layer that completely fills the aperture; and

planarizing a backside of the substrate to expose at least the conformal conductor layer.

18. The method of claim 17 wherein the forming the blind aperture provides the blind aperture with a linewidth from about 5 to about 15 microns and an aspect ratio from about 10:1 to about 30:1.

19. The method of claim 17 wherein the planarizing the backside exposes the conformal conductor layer but not the plug layer.

20. The method of claim 17 wherein the planarizing the backside exposes the conformal conductor layer and the plug layer.

21. The microelectronic structure of claim 8, wherein the plug layer is a dielectric having a void present therein.

22. A method for fabricating a microelectronic structure comprising:

forming a blind aperture within a substrate;

depositing within the blind aperture a conformal conductor layer that does not completely fill the blind aperture, a conformal planarization stop layer on a base and sidewalls of the conformal conductive layer and a plug layer that does completely fill the blind aperture with said plug layer having a void present therein; and

planarizing a backside of the substrate to contact at least the conformal conductor layer, wherein a planarized surface of the substrate is coplanar with a planarized surface of the conformal conductor layer, a planarized surface of the conformal planarization stop layer and a planarized surface of the plug layer.

23. The method of claim 22 wherein the forming of the blind aperture provides; the blind aperture with a linewidth from about 5 to about 15 microns and an aspect ratio from about 1:10 to about 1:30.

24. The method of claim 22 further comprising depositing a conformal liner layer into the blind aperture prior to depositing the conformal conductor layer.

25. The method of claim 22 wherein the successive layering further comprises successive layering a conformal stop layer after successive layering the conformal conductor layer and prior to successive layering the plug layer.

26. The method of claim 22 wherein the planarizing the backside exposes the conformal conductor layer and the plug layer.

27. The method of claim 22 further comprising forming a conductor layer over the substrate and contacting a planarized conformal conductor layer.

28. The method of claim 22 further comprising forming a conductor layer under the substrate and contacting the planarized conformal conductor layer.

29. A method for fabricating a microelectronic structure comprising:

forming a blind aperture having side and bottom surfaces within a semiconductor substrate having top and backsides thereof;

depositing within the blind aperture, along the side and bottom surfaces thereof, a conformal dielectric liner layer of a selected thickness that has side and bottom surfaces and that does not completely fill the blind aperture,

depositing a conformal conductor layer of a selected thickness that has side and bottom surfaces within the conformal dielectric liner layer that does not completely fill the blind aperture,

depositing a conformal planarization stop layer of a selected thickness that has side and bottom surfaces within the conformal conductor layer that does not completely fill the blind aperture and

depositing a plug layer within the conformal planarization stop layer that does completely fill the blind aperture with said plug layer having a void present therein; and

planarizing the backside of the substrate to contact at least the conformal conductor layer in an annular geometry, wherein the planarizing stops on a base portion of the bottom surface of the planarization stop layer centrally positioned within the annular geometry of the

conformal conductor layer, wherein a planarized surface of the substrate is coplanar with a planarized surface of the conformal conductor layer and a planarized surface of the base portion of the bottom surface of the planarization stop layer.

30. The method of claim 29 wherein the forming the blind aperture provides the blind aperture with a linewidth from about 5 to about 15 microns and an aspect ratio from about 10:1 to about 30:1.

31. The method of claim 29 wherein the planarizing the backside exposes the conformal conductor layer but not the plug layer.

32. The method of claim 29 wherein the planarizing the backside exposes the conformal conductor layer and the plug layer.

33. A method for fabricating a microelectronic structure comprising:

forming a blind aperture within a semiconductor substrate;

depositing within the blind aperture a conformal dielectric liner layer that does not completely fill the blind aperture, a conformal conductor layer that does not completely fill the blind aperture, a conformal planarization stop layer that does not completely fill the blind aperture and a plug layer that does completely fill the blind aperture with said plug layer having a void present therein; and

planarizing a backside of the substrate to contact at least the conformal conductor layer, wherein the planarized surface of the substrate is coplanar with a planarized surface of the conformal conductor layer, a planarized surface of the conformal planarization stop layer and a planarized surface of the plug layer.

34. The method of claim 33 wherein the forming the blind aperture provides the blind aperture with a linewidth from about 5 to about 15 microns and an aspect ratio from about 10:1 to about 30:1.

35. The method of claim 33 wherein the planarizing the backside exposes the conformal conductor layer but not the plug layer.

36. The method of claim 33 wherein the planarizing the backside exposes the conformal conductor layer and the plug layer.