

ABSTRACT

A chip stack package includes a first semiconductor chip having a first test bump on a first surface and a second semiconductor chip
5 stacked on a second surface of the first semiconductor chip opposite the first surface. The chip stack package also includes a second test bump bonded to the first test bump. The chip stack package further includes a mold member surrounding the first semiconductor chip, the second semiconductor chip, and the second test bump. The chip stack
10 package additionally includes a test pad disposed on the mold member and connected to the second test bump.

FIG. 1