# PROCESS FLOW FOR A PERFORMANCE ENHANCED MOSFET WITH SELF-ALIGNED, RECESSED CHANNEL

## ABSTRACT

A method for forming a self-aligned, recessed channel, MOSFET device that alleviates the problems due to short channel and hot carrier effects while reducing inter-electrode capacitance is described. A substrate with an active area encompassed by a shallow trench isolation (STI) region is provided. A gate recess is formed in the substrate. A tapered oxide layer is formed along the sidewalls of the gate recess. A threshold adjust and punch-through implantation is performed into the substrate below the gate recess. The oxide layer at the bottom of the gate recess is removed and a gate dielectric layer is grown in the bottom of the gate recess. Gate polysilicon fills the gate recess. A screen oxide layer is then deposited, followed by light and heavy S/D implantations and annealing. Metallization and passivation complete the fabrication of the MOS transistor device.

FIG 12A and FIG 12B