

CORRECTED VERSION

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
8 February 2007 (08.02.2007)

PCT

(10) International Publication Number
WO 2007/016168 A1

(51) International Patent Classification:
H04N 3/15 (2006.01)

(21) International Application Number:
PCT/US2006/029050

(22) International Filing Date: 26 July 2006 (26.07.2006)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
11/193,322 1 August 2005 (01.08.2005) US

(71) Applicant (for all designated States except US): **MICRON TECHNOLOGY, INC.** [US/US]; 8000 S. Federal Way, Boise, ID 83707-0006 (US).

(72) Inventor; and

(75) Inventor/Applicant (for US only): **MCKEE, Jeffrey, A.** [US/US]; 3891 S. Gideon Place, Meridian, ID 83642 (US).

(74) Agent: **D'AMICO, Thomas, J.**; Dickstein Shapiro LLP, 1825 Eye Street, NW, Washington, DC 20006-5403 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM,

AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LV, LY, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

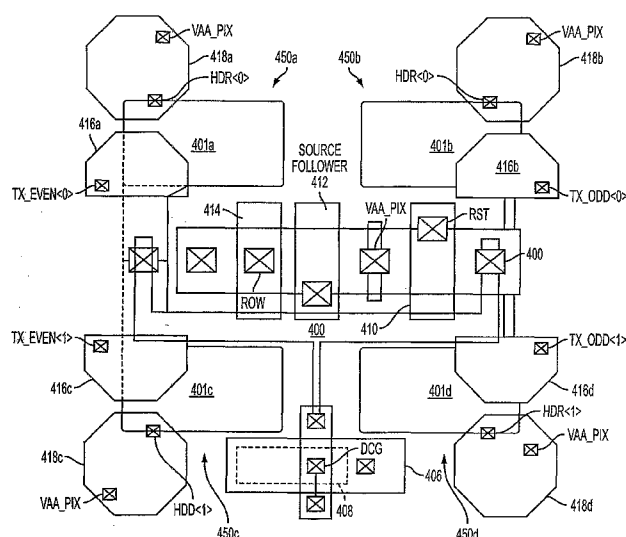
— with international search report

(48) Date of publication of this corrected version:

27 March 2008

(15) Information about Correction:
see Notice of 27 March 2008

(54) Title: DUAL CONVERSION GAIN GATE AND CAPACITOR COMBINATION



(57) Abstract: A pixel cell array architecture having a dual conversion gain. A dual conversion gain element is coupled between a floating diffusion region and a respective storage capacitor. The dual conversion gain element having a control gate switches in the capacitance of the capacitor to change the conversion gain of the floating diffusion region from a first conversion gain to a second conversion gain. In order to increase the efficient use of space, the dual conversion gain element gate also functions as the bottom plate of the capacitor. In one particular embodiment of the invention, a high dynamic range transistor is used in conjunction with a pixel cell having a capacitor-DCG gate combination; in another embodiment, adjacent pixels share pixel components, including the capacitor-DCG combination.

WO 2007/016168 A1