

CAPACITOR-LESS FLOATING-BODY VOLATILE MEMORY CELL COMPRISING A PASS TRANSISTOR  
AND A VERTICAL READ/WRITE ENABLE TRANSISTOR AND MANUFACTURING AND PROGRAMMING  
METHODS THEREOF

PRIORITY CLAIM

5           This application claims the benefit of the filing date of United States Patent  
Application Serial No. 11/711,449 filed February 26, 2007, for  
“CAPACITOR-LESS VOLATILE MEMORY CELL, DEVICE, SYSTEM AND  
METHOD OF MAKING SAME.”

## 10 TECHNICAL FIELD

Various embodiments of the present invention relate generally to the field of volatile memory devices and, more particularly, to capacitor-less memory cells.

## BACKGROUND

15 A widely-utilized DRAM (Dynamic Random Access Memory) manufacturing process utilizes CMOS (Complementary Metal Oxide Semiconductor) technology to produce DRAM circuits which comprise an array of unit memory cells, each including one capacitor and one transistor, such as a field effect transistor. In the most common circuit designs, one side of the transistor is  
20 connected to one side of the capacitor, the other side of the transistor and the transistor gate are connected to external circuit lines called the digit line and the word line, and the other side of the capacitor is connected to a reference voltage. In such memory cells, an electrical signal charge is stored in a storage node of the capacitor connected to the transistor that charges and discharges the circuit lines of  
25 the capacitor.

Higher performance, lower cost, increased miniaturization of components, and greater packaging density of integrated circuits are ongoing goals of the computer industry. In pursuit of increased miniaturization, DRAM chips have been continually redesigned to achieve ever higher degrees of integration. However, as the dimensions of the DRAM chips are reduced, the occupation area of each unit memory cell of the DRAM chips must be reduced. This reduction in occupied area necessarily results in a reduction of the dimensions of the capacitor, which, in turn,

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makes it difficult to ensure required storage capacitance for transmitting a desired signal without malfunction. However, the ability to densely pack the unit memory cells, while maintaining required capacitance levels, results in the necessity to build taller or deeper capacitors in order to maintain adequate charge storage for adequate data retention. Accordingly, taller or deeper capacitors results in aspect ratios that require expensive processes and result in increased opportunities for defects.

Specialized fabrication processes unique to the formation of large aspect ratio devices such as capacitors do not lend themselves to being integrated with logic devices such as controllers or processors. Therefore, it would be advantageous to develop a data storage cell capable of high density fabrication while not utilizing overly peculiar processing steps that are incompatible with logic device fabrication techniques.

#### DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross section of a formation of a structure, in accordance with an embodiment of the present invention.

FIG. 2 is a cross section of a further formation of the structure of FIG. 1, in accordance with an embodiment of the present invention.

FIG. 3 is a cross section of a further formation of the structure of FIG. 2, in accordance with an embodiment of the present invention.

FIG. 4 is a cross section of a further formation of the structure of FIG. 3, in accordance with an embodiment of the present invention.

FIG. 5 is a cross section of a further formation of the structure of FIG. 4, in accordance with an embodiment of the present invention.

FIG. 6 is a cross section of a further formation of the structure of FIG. 5, in accordance with an embodiment of the present invention.

FIG. 7 is a cross section of a further formation of the structure of FIG. 6, in accordance with an embodiment of the present invention.

FIG. 8 is a cross section of a further formation of the structure of FIG. 7, in accordance with an embodiment of the present invention.

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FIG. 9 is a cross section of a further formation of the structure of FIG. 8, in accordance with an embodiment of the present invention.

FIG. 10 is a cross section of a further formation of the structure of FIG. 9, in accordance with an embodiment of the present invention.

5        FIG. 11 is a cross section of a further formation of the structure of FIG. 10, in accordance with an embodiment of the present invention.

FIG. 12 is a circuit diagram of a capacitor-less memory cell, in accordance with an embodiment of the present invention.

10       FIG. 13 is a block diagram of a memory device, in accordance with an embodiment of the present invention.

FIG. 14 is a block diagram of an electronic system, in accordance with an embodiment of the present invention.

FIG. 15 is a block diagram of an electronic system, in accordance with another embodiment of the present invention.

15       FIG. 16 is a diagram of a semiconductor wafer including an integrated circuit die incorporating a memory cell of one or more of the previous embodiments, in accordance with a further embodiment of the present invention.

#### MODE(S) FOR CARRYING OUT THE INVENTION

20       In the following detailed description, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be implemented, and that structural, logical and electrical changes may be made without departing  
25       from the spirit and scope of the present invention.

Embodiments of a capacitor-less memory cell, memory device, system and process of forming the capacitor-less memory cell are disclosed. The capacitor-less memory cell is formed according to a partial silicon-on-insulator (SOI) technique,  
30       wherein the active area is formed from a substantially physically isolated portion of the bulk semiconductor substrate. A pass transistor is formed on the active area and

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includes a pass transistor including a source region and a drain region for coupling with a digit line. A gate of the pass transistor is configured for coupling with a word line. The capacitor-less memory cell further includes a read/write enable transistor including a gate, a source region and a drain region commonly shared with the source region of the pass transistor. The read/write enable transistor is vertically configured along at least one vertical side of the active area and activated, or operable, during a reading of a logic state with the logic state being stored as charge in a floating body area of the active area, causing different determinable threshold voltages for the pass transistor.

10           An embodiment of a process for forming a capacitor-less memory cell is also disclosed. The process includes etching an active area from a bulk semiconductor substrate with the active area being substantially physically isolated from the bulk semiconductor substrate in a partial SOI process. A read/write enable transistor is formed and includes a gate, a source region and a drain region commonly shared with the source region of the pass transistor. The read/write enable transistor is vertically configured along at least one vertical side of the active area and configured to be activated, or operable, during a reading of a logic state. The process further includes forming a pass transistor in the active area with the pass transistor including a source region, a drain region for coupling with a digit line and a gate for coupling with a word line. A logic state is stored as charge in a floating body area of the active area, causing different determinable threshold voltages for the pass transistor.

25           An embodiment of a memory device is also disclosed, which embodiment includes a memory array including a plurality of capacitor-less memory cells. Each of the plurality of capacitor-less memory cells includes an active area formed from a substantially physically isolated portion of a bulk semiconductor substrate with a pass transistor formed on the active area. The pass transistor includes a source region, a drain region for coupling with a digit line and a gate for coupling with a word line. Each of the plurality of capacitor-less memory cells further includes a read/write enable transistor including a gate, a source region and a drain region commonly shared with the source region of the pass transistor. The read/write enable transistor is vertically configured along at least one vertical side of the active

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area and activated, or operable, during a reading of a logic state with the logic state being stored as charge in a floating body area of the active area, causing different determinable threshold voltages for the pass transistor. The memory device also includes addressing and sensing circuitry coupled to the memory array and  
5 configured to select and read and write to selected ones of the plurality of capacitor-less memory cells.

An embodiment of a semiconductor wafer including at least one memory device including a plurality of capacitor-less memory cells thereon is also disclosed.

Embodiments of electronic systems including input, output, processor and  
10 memory devices are also disclosed. In one embodiment of the present invention, the electronic system includes the input, output, processor and memory devices operably coupled together. In another embodiment of the present invention, the input, output, and processor devices are operably coupled together and the memory device is integrated into the processor device. The capacitor-less memory cells are further  
15 formed and configured as described herein.

In one embodiment as depicted in FIG. 1, a substrate 10 is provided which includes a semiconductive material. The terms "wafer" and "substrate" used in the following description include any structure having an exposed surface, on or in which an integrated circuit (IC) structure relating to embodiments of the present  
20 invention may be formed. The term substrate includes, without limitation, semiconductor wafers. The term substrate is also used to refer to semiconductor structures during processing, and may include other layers that have been fabricated thereupon. Both wafer and substrate include doped and undoped semiconductors, epitaxial semiconductor layers supported by a base semiconductor or insulator, as  
25 well as other semiconductor structures known to one skilled in the art. The term "conductor" includes semiconductors, and the term "insulator" or "dielectric" includes any material that is less electrically conductive than the materials referred to as conductors.

The illustrated portion of the substrate 10 may also be a portion of an  
30 implanted "tub" region of, for example, a p-type doped region of a differently doped greater substrate. The substrate 10 has an implant region 12 formed through ion

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implantation into the substrate 10 according to conventional implant techniques, including masking, to form an implant region that is offset in one direction as illustrated and, in one embodiment, implant region 12 is formed to result in an n-type region. The substrate 10 also includes a pad oxide layer 14 deposited thereon.

5 As used herein, the term deposited is used broadly to mean layers which are not only deposited in the traditional sense, but layers of material which are grown or in any other manner caused to be formed. A protective layer 16 is deposited on top of the pad oxide layer 14 to act as a buffer during subsequent etch steps and other processing. In one embodiment, the protective layer 16 is polysilicon. In another  
10 embodiment, the protective layer 16 is a nitride material. In yet another embodiment, the protective layer 16 is a polysilicon layer that is covered with a nitride material. The specific combination is selected depending upon process integration choices.

A mask 18 is formed and patterned upon the protective layer 16. In one  
15 embodiment, the mask 18 is a photoresist material that is spun on, exposed, cured, and patterned. In another embodiment, the mask 18 is a hard mask material such as a nitride or oxide. The area protected by the mask 18 defines what will become an active area in a partial silicon-on-insulator (SOI) structure used to form a capacitor-less memory cell.

20 FIG. 2 illustrates an embodiment after an etch process that has exposed the regions unprotected by the mask 18. In the etch process, the protective layer 16 and the pad oxide layer 14 have also been patterned, and a recess 20 has been formed with a recess first bottom 22 and an upper first wall 24 and an upper second wall 26. It should be noted that only a cross section of the structure is illustrated in  
25 FIGs. 1-11 and therefore upper third and fourth walls are not illustrated but are located on adjacent sides of upper first wall 24 and upper second wall 26.

FIG. 3 illustrates the structure depicted in FIG. 2 after further processing in which the mask 18 has been removed and a nitride film 28 has been grown onto the exposed semiconductive material of the substrate 10. In one embodiment, the  
30 exposed semiconductive material of the substrate 10 is exposed silicon. The nitride film 28 is depicted as covering the recess first bottom 22, the upper first wall 24 and

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upper second wall 26. The nitride film 28 may be grown by known processes under conditions that deposit only upon semiconductive material such as exposed silicon. One such process is remote-plasma nitridation (RPN). In RPN, a nitride-bearing plasma is struck, remote from substrate 10, but within the deposition tool, and the nitride-bearing plasma is carried by convective force toward the substrate 10. Another process that may be used to form the nitride film 28 is rapid thermal nitridation (RTN). Such processing is also known in the art.

Alternative to the formation of a nitride film 28, an oxide film may be formed, either by remote-plasma oxidation (RPO) or by rapid thermal oxidation (RTO) or in situ steam generation (ISSG) or low pressure radical oxidation (LPRO). Similarly, a combination of an oxide and a nitride is formed according to an embodiment as set forth herein. In one embodiment, the placement of the oxide precedes the placement of the nitride, or visa versa. Similarly, an oxynitride film is formed in the place of the nitride film 28 according to an alternative embodiment. The process is carried out by either a remote plasma process or a rapid thermal process. Although not limiting the embodiments disclosed, for convenience throughout the remainder of the disclosure, the film 28 is referred to as the nitride film 28.

FIG. 4 illustrates processing of the substrate 10 in which an etch has formed a recess second bottom 30 below the level of the recess first bottom 22 and at about the depth of the implant region 12. The recess first bottom 22 now appears as a substrate ledge structure. Because of the presence of the nitride film 28, the upper first wall 24, upper second wall 26, and upper third and fourth walls (not shown) are protected, and a lower wall 32 has been formed that is approximately coplanar with the lateral extremity of the nitride film 28. In one embodiment, an anisotropic etch, such as a reactive ion etch, is used such that the nitride film 28 is left standing upon the ledge of what is left of the recess first bottom 22.

For a 0.25-micron critical-dimension (CD or minimum feature) process, the remnant of the nitride film 28 has a height in a range from about 0.1 microns to about 0.15 microns. In this dimension, the distance from the remnant of the recess first bottom 22 to the recess second bottom 30 is in a range from about 0.1 microns

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to about 0.3 microns. Alternatively, for a 0.15-micron critical-dimension (CD or minimum feature) process, the remnant of the nitride film 28 has a height, H, in a range from about 0.07 microns to about 0.12 microns. In this dimension, the distance from the remnant of the recess first bottom 22 to the recess second

5 bottom 30 is in a range from about 0.08 microns to about 0.2 microns.

At the level of the recess second bottom 30, a deep implantation region 34 is formed. In one embodiment, the deep implantation region 34 is made of materials that are substantially identical to the bulk semiconductive material in the substrate 10. Implantation is carried out at an energy level that achieves

10 self-interstitial implantation, and that causes the implantation region 34 to become amorphous enough to have an etch responsiveness that is different from the bulk semiconductive material in the substrate 10. In one embodiment, implantation conditions use a silicon source that is implanted to a monocrystalline-to-self interstitial ratio of about 3:1. By "silicon source" it is meant that silicon or another  
15 Group IV element is used, or a combination such as silicon and germanium. In one embodiment, the implanted concentration is from about  $1\text{E}^{14}$  atoms/cm<sup>2</sup> to about  $5\text{E}^{15}$  atoms/cm<sup>2</sup> at process conditions of ambient temperature (20 C. to about 30 C.) and an implantation energy from about 500 eV to about 30 KeV. In one embodiment, a silicon source that is substantially equivalent to the silicon chemistry  
20 of the bulk of the semiconductive substrate 10, is implanted to a concentration of about  $1\text{E}^{15}$  atoms/cm<sup>2</sup> and process conditions are about 25 C. and an implantation energy of about 25 KeV. In another embodiment, the implantation energy may be on the order of about 1 KeV.

After the deep implantation, an etch process is used in subsequent processing  
25 that is selective to the amorphous material of the implantation region 34 and to the nitride film 28, but the etch process removes bulk semiconductive material in the substrate 10. In one embodiment, the etch process is a wet tetramethyl ammonium hydroxide (TMAH) etch as is known in the art. In another embodiment, the wet etch uses a potassium hydroxide (KOH) etch chemistry that is known in the art. The  
30 TMAH etch chemistry is desirable because it is selective such that it etches the bulk silicon of the substrate 10, but does not substantially etch the nitride film 28 or the

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deep implantation region 34. In one embodiment, the selectivity is in a range from about 5:1 to about 20:1. In another embodiment, the selectivity is about 10:1. The isotropic etch may also be combined with an anisotropic etch, either before or after the isotropic etch. By using both an isotropic and an anisotropic etch, both the  
5 downward etching and the undercutting of the nitride film 28 may be varied to suit particular applications.

Various wet TMAH etch processes are known that are selective to amorphous silicon and to nitride films (or oxide films, or oxynitride films), and that isotropically etch bulk monocrystalline silicon along crystallographic planes. FIG. 5  
10 illustrates the results of a TMAH etch that has formed a lateral cavity 38 that has undercut what will become the active area 36. By this undercutting etch, the active area 36 has been mostly isolated from the bulk semiconductive material in the substrate 10, at the level of the ledge that is formed at the recess first bottom 22.

Under the etch conditions, and due to the scale of the lateral cavity 38, a  
15 distinctive contour is formed therein. The TMAH etch has an effect along crystallographic planes such that a faceted contour may appear within the lateral cavity 38. Accordingly, faceted surface 44 is illustrated on one side. However, these are depicted in arbitrary shape, angle and size for illustrative purposes, and the specific shapes, angles, and sizes of the faceted surfaces will depend upon the  
20 crystallographic orientation of the bulk semiconductive material in the substrate 10 and upon the specific etch process and conditions, among other factors. According to the specific etch conditions, a photomicrographic view of the lateral cavity 38 depicts subtended crystallographic planes of bulk semiconductive material in the substrate 10 that have been exposed by the TMAH etch. It should be noted that  
25 there are other various methods for forming the lateral cavity 38 which are also contemplated to be within the scope of the present invention.

After formation of the lateral cavity 38, the implantation region 34 is treated to form an annealed implantation region 46 as illustrated in FIG. 6. The annealed implantation region 46 has been returned to substantially the same semiconductive  
30 quality as the bulk semiconductive material in the substrate 10 by substantially repairing the monocrystalline lattice in what was the deep implantation region 34

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(FIG. 5). The conditions for annealing are known in the art, and depend upon the depth of the deep implantation region 34, the available thermal budget of the process, and other factors.

FIG. 7 illustrates further processing according to an embodiment. In one embodiment, the exposed surface of the active area 36 and the bulk semiconductive material of the substrate 10 is oxidized, in one embodiment, using minimal conditions. The minimal oxidation conditions relates to a lowered workpiece stress in the lateral cavity 38. An oxidation 48, such as a shallow trench isolation (STI) oxide, is formed that provides a thin oxide layer. The oxidation 48 consumes silicon downward into the substrate 10, sideways into the faceted area 44 (FIG. 6), and upward into bottom of the active area 36. In one photolithographic process, such as a 0.25-micron process, the dimensions are about 0.03 microns growth of oxidation 48 toward the remaining portion of the substrate stem 52. In another photolithographic process, such as a 0.15-micron process, the dimensions are about 0.01 microns toward the substrate stem 52 that remains to this stage of processing.

FIG. 7 also depicts the protective layer 16 remaining while the nitride film 28 has been removed. This embodiment occurs where the protective layer 16 is chemically different from the nitride film 28, such as a polysilicon protective layer 16. In another embodiment, where the protective layer 16 is a nitride material, it is removed with the nitride film.

For one photolithographic process, the amount of the substrate 10 that is consumed sideways by the isotropic etch, for example, is approximately 0.07 micron on each side of the active area 36. That oxidation process leaves the substrate stem 52 that connects the substrate that will become the active area 36 to the bulk of the substrate 10. In this embodiment, the substrate stem 52 is on the order of about 0.05 microns by 0.05 microns. Oxidation time will depend upon the area of the partially isolated structure that forms the active area 36 and the other parameters. In one embodiment, oxidation parameters include a processing temperature from about 850° C. to about 1,100° C. The ambient is with wet or dry oxygen (O<sub>2</sub>) or radicals or ozone, atmospheric pressure or higher. In one example, a temperature of about 850° C. and a wet oxygen ambient is applied for a sufficient time to allow about 0.03

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micron horizontal oxidation under the active area 36, and about 0.01 micron vertical oxidation upwardly into the active area 36. After the thermal oxidation process, oxidation is formed to fill lateral cavity 38 and provide support and isolation to the active area 36 supported by substrate stem 52.

5           In one embodiment, a first oxide 40 is formed for filling the lateral cavity 38. The first oxide 40 may be formed of a spin-on dielectric (SOD) material, high-density plasma (HDP) oxide material or other dielectric fill. When a SOD material is desired, the layer 48 may be configured as a nitride and oxide combination layer to allow the proper densification of the SOD material. By way of  
10       example, spin-on dielectric oxide (SOD) material provides good oxidation for trenches or cavities, such as lateral cavity 38, that are formed according to sub-micron dimensions. The spin-on dielectric (SOD) process entails dripping a liquid precursor onto the wafer surface in a predetermined amount. The wafer is subjected to rapid spinning (e.g., up to 6000 rpm). The spinning uniformly  
15       distributes the liquid on the surface by centrifugal forces allowing low points to be filled. Finally, the coating is baked in order to solidify the material. Further details of spin-on dielectric (SOD) processes are known by those of ordinary skill in the art and may include processes described in U.S. Patent No. 7,112,513. In yet another embodiment, a TEOS material may be used instead of a SOD material. Furthermore,  
20       combinations of the oxide materials are also contemplated.

          While a continuous fill of oxide material into the cavity 38 for forming a planar isolation to the protective layer 16 is contemplated, the present embodiment illustrates a second oxide 42 formed by an oxidation process (e.g., high-density plasma (HDP) oxide material, spin-on dielectric (SOD) material or other dielectric  
25       fill). The second oxide 42 may contain the same dielectric material or a dielectric material different from the first oxide 40. Since the lateral cavity 38 has been filled by the first oxide 40, the second oxide 42 may be formed according to more aggressive oxidation processes.

          FIG. 8 illustrates further processing according to an embodiment of the  
30       present invention. A mask 50 is formed and patterned upon the protective layer 16 and the second oxide 42 on one side of the active area 36. In one embodiment, the

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mask 50 is a photoresist material that is spun-on, exposed, cured, and patterned. The mask 50 protects one or more sides of the active area 36 from process steps occurring on at least one other side of active area 36. The mask 50 provides protection from removal of the first oxide 40 and second oxide 42 on at least one  
5 side of the active area 36. An etching process exposes the regions unprotected by the mask 50. In the present etch process, the protective layer 16 and the mask 50 allow the first oxide 40' and the second oxide 42' to be removed for the formation of a vertical gate along at least one side of the active area 36.

FIG. 9 illustrates further processing according to an embodiment of the  
10 present invention. A minimal oxidation in the form of gate oxide 54 is formed along an open upper second wall 26 of active area 36 and along an open cavity wall 56 of substrate stem 52. The continuous gate oxide 54 allows for the formation of a vertical transistor along active area 36 and substrate stem 52. A conductive material 60 is formed over the gate oxide 54 to create the vertical gate 58 on at least  
15 one side of the substrate stem 52. Furthermore, an n-type junction extension 61 is diffused from the poly fill area which results in providing a desirable electrical contact between conductive material 60 and the implant region 12. In one embodiment, conductive material 60 (e.g., polysilicon or metal) forms a continuous conductor along the z-direction (i.e., into and out of the illustrated figure and parallel  
20 with the word line which is perpendicular with the digit line) for coupling with the read/write enable signal 62. Furthermore, the proximity of adjacent memory cells may be reduced by placing a single contact at the end of the continuous conductor of the read/write enable signal 62.

FIG. 10 illustrates further processing of the structure, according to an  
25 embodiment of the present invention. The active area 36 is implanted according to mask 64 to form a first drain region 66 and first source region 68, configured as a floating source region, of a forthcoming pass transistor 70. The pass transistor 70 is gated by a word line and the first drain region 66 is connected to a digit line for reading and writing by a sense amplifier (not shown). The active area 36 is further  
30 implanted according to mask 72 to form a second drain region 74 which, in combination with first source region 68, forms the drain region, referred to hereafter

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as a common region 80, for the vertically configured read/write enable transistor 76. A second source region 78 for the vertically configured read/write enable transistor 76 results from the implant region 12.

FIG. 11 illustrates further processing of the structure, according to an embodiment of the present invention. A capacitor-less memory cell 82 including a pass transistor 70 and a read/write enable vertical transistor 76 is formed on the active area 36 according to a partial SOI process. The pass transistor 70 at the first drain region 66 couples to a digit line 84 and at the gate 86 couples to the word line 88. The source region of the pass transistor 70 is configured as a floating source at common region 80. The vertically configured read/write enable transistor 76 includes the vertical gate 58, a drain region located at the common region 80 and the second source region 78 resulting from implant region 12 (FIG. 1). The vertical gate 58 couples to the read/write enable signal 62 which is activated during reading of the capacitor-less memory cell 82.

FIG. 12 illustrates a circuit diagram of the capacitor-less memory cell, in accordance with an embodiment of the present invention. The capacitor-less memory cell 82 is illustrated to include pass transistor 70 coupled with the read/write enable transistor 76. The various control signals, namely word line 88 and read/write enable signal 62 respectively control the gates of the pass transistor 70 and the read/write enable transistor 76. The digit line 84 is coupled to the first drain region 66 of pass transistor 70. A bipolar junction transistor (BJT) 90 is also illustrated as the dominant parasitic device. In general, information is stored in the capacitor-less memory cell by charging or discharging the channel region of the pass transistor 70. The channel region of the pass transistor 70 is isolated according to the partial SOI process described hereinabove and in addition to the gated-diode configuration of the read/write enable transistor 76. Such a configuration results in a low leakage from the channel region and accommodates charge storage in the channel region.

During operation when the capacitor-less memory cell is neither being written to or read from, the read/write enable signal 62 is set at less than the threshold voltage of the vertical read/write enable transistor 76 but greater than the

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VBE of about, for example, 0.55 V. First and second logic states are written into the capacitor-less memory cell according to charge stored in the floating body region 92 (FIGs. 11 and 12).

A first logic state, such as a low logic state, is written into the capacitor-less memory cell by storing charge in the floating body region 92. The charging of the floating body region 92 occurs when the read/write enable transistor 76 is turned off by applying a negative voltage (e.g., about -0.6V to -1V) as the read/write enable signal 62. The p-type substrate 10 is set to 0V or allowed to float. This condition results in low conduction through the pass transistor 70 during a read operation since the threshold voltage of the pass transistor is higher (e.g., about +1V) and further since the  $V_{BB} \ll V_{BE}$  as charge has been added to the floating body region 92.

A second logic state, such as a high logic state, is written into the capacitor-less memory cell by depleting or discharging the charge from the floating body region 92. Discharging occurs when the read/write enable transistor 76 is turned off by applying a positive voltage (e.g., about +0.6V) to the read/write enable signal 62 and applying a positive voltage (e.g., about +1V) to the p-type substrate 10. This condition results in a high conduction through the pass transistor 70 during a read operation since the threshold voltage of the pass transistor is lower (e.g., about 0.2V) and further since the  $V_{BB} \approx V_{BE} - 0.1V$  as charge has been discharged from the floating body region 92.

During a read operation of the capacitor-less memory cell, the logic state is read to the digit line 84 when the word line 88 is high (i.e., between the threshold voltage of the pass transistor indicating a high logic state and the threshold voltage of the pass transistor indicating a low logic state). Additionally, the read/write enable transistor 76 is turned on by applying a voltage to the read/write enable signal 62 that is greater than the threshold voltage of the read/write enable transistor 76 and the p-type substrate 10 is floating.

Since there is finite leakage in the floating body region 92, adequate electron concentrations must be maintained in order to preserve the stored logic states. Therefore, the capacitor-less memory cell may be characterized as a form of a Dynamic Random Access Memory (DRAM). Accordingly, refresh operations need

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to be periodically performed with the period being determined based upon the specific processes implemented.

FIG. 13 is a block diagram of a memory device, in accordance with an embodiment of the present invention. A DRAM memory device 100 includes control logic circuit 120 to control read, write, erase and perform other memory operations. A column address buffer 124 and a row address buffer 128 are adapted to receive memory address requests. A refresh controller/counter 126 is coupled to the row address buffer 128 to control the refresh of the memory array 122. A row decode circuit 130 is coupled between the row address buffer 128 and the memory array 122. A column decode circuit 132 is coupled to the column address buffer 124. Sense amplifiers-I/O gating circuit 134 is coupled between the column decode circuit 132 and the memory array 122. The DRAM memory device 100 is also illustrated as having an output buffer 136 and an input buffer 138. An external processor may be coupled to the control logic circuit 120 of the DRAM memory device 100 to provide external commands.

A capacitor-less memory cell 150 of the memory array 122 is shown in FIG. 13 to illustrate how associated memory cells are implemented in the present invention. States or charges are stored in the capacitor-less memory cell 150 that correspond to a data bit. A word line WL0 142 is coupled to the gate of the pass transistor of the capacitor-less memory cell 150. When the word line WL0 142 is activated, the charge stored in the capacitor-less memory cell causes a determinable amount of current to flow or to not flow to the digit line DL0 152 based upon the logic state stored in the capacitor-less memory cell. Digit line DL0 152 is coupled to a sense amplifier in circuit 134.

FIG. 14 is a block diagram of an electronic system, in accordance with an embodiment of the present invention. The electronic system 200 includes an input device 272, an output device 274, and a memory device 278, all coupled to a processor device 276. The memory device 278 incorporates at least one capacitor-less memory cell 240 of one or more of the preceding embodiments of the present invention.

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FIG. 15 is a block diagram of an electronic system, in accordance with another embodiment of the present invention. The electronic system 300 includes an input device 272, an output device 274, and a processor device 376 incorporating therein a memory device 378 includes at least one capacitor-less memory cell 340.

- 5 As stated, the disclosed capacitor-less memory cell implemented using a partial SOI process does not require the process fabrication steps for forming large data retention capacitors. Therefore, the fabrication processes for forming the capacitor-less memory device according to the embodiments described herein are compatible with the fabrication processes for forming logic devices such as a processor device.
- 10 Accordingly, a memory device incorporating the capacitor-less memory cell described herein may be integrated onto the processor die for close integration.

- FIG. 16 is a diagram of a semiconductor wafer including an integrated circuit die incorporating the memory array and capacitor-less memory cells of one or more of the previous embodiments, in accordance with a further embodiment of the present invention. As shown in FIG. 16, a semiconductor wafer 400 includes a yet-to-be cut integrated circuit die 440 that incorporates one or more capacitor-less memory cells as herein disclosed.
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- The processes and devices described above illustrate embodiments of methods and devices out of many that may be used and produced according to the embodiments of the present invention. The above description and drawings illustrate embodiments which provide significant features and advantages of the present invention. It is not intended, however, that the present invention be strictly limited to the above-described and illustrated embodiments.
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- Although the present invention has been shown and described with reference to particular embodiments, various additions, deletions and modifications that will be apparent to a person of ordinary skill in the art to which the invention pertains, even if not shown or specifically described herein, are deemed to lie within the scope of the invention as encompassed by the following claims.
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## CLAIMS

What is claimed is:

- 5           1.       A capacitor-less memory cell, comprising:  
an active area formed from a substantially physically isolated portion of a bulk  
semiconductor substrate;  
a pass transistor formed on the active area, the pass transistor including a source  
region, a drain region for coupling with a digit line and a gate for coupling  
10           with a word line; and  
a read/write enable transistor including a gate, a source region, and a drain region  
commonly shared with the source region of the pass transistor, the read/write  
enable transistor vertically configured along at least one vertical side of the  
active area and operable during a reading of a logic state, the logic state being  
15           storable as charge in a floating body area of the active area to cause different  
determinable threshold voltages for the pass transistor.
- 20           2.       The capacitor-less memory cell of claim 1, wherein the active area  
remains physically integrally connected with the bulk semiconductor substrate  
through a stem portion of the bulk semiconductor substrate.
- 25           3.       The capacitor-less memory cell of claim 2, wherein at least a portion  
of the gate of the read/write enable transistor is formed along at least one side of the  
stem portion connecting the active area and the bulk semiconductor substrate.
- 30           4.       The capacitor-less memory cell of claim 3, further comprising  
isolating oxide between at least another one side of the stem portion and the bulk  
semiconductor substrate.
5.       The capacitor-less memory cell of claim 3, wherein the source of the  
read/write enable transistor is formed in the bulk semiconductor substrate.

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6. The capacitor-less memory cell of claim 5, wherein the source of the read/write enable transistor is formed under the stem portion in the bulk semiconductor substrate.

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7. The capacitor-less memory cell of claim 1, wherein the commonly shared source region of the pass transistor and the drain region of the read/write enable transistor substantially extends through the thickness of the active area.

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8. The capacitor-less memory cell of claim 1, wherein the floating body area of the active area is configured to be more negatively charged to represent a first logic state and the floating body area is configured to be less negatively charged to represent a second logic state.

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9. A process of forming a capacitor-less memory cell, comprising:  
etching an active area from a bulk semiconductor substrate and to be substantially physically isolated from the bulk semiconductor substrate;  
forming a read/write enable transistor adapted to be operable during a reading of a logic state, vertically configured along at least one vertical side of the active area and including a gate, a source region, and a drain region commonly shared with the source region of the pass transistor; and  
forming a pass transistor in the active area, the pass transistor including a source region, a drain region for coupling with a digit line and a gate for coupling with a word line, wherein the logic state is storable as charge in a floating body area of the active area to cause different determinable threshold voltages for the pass transistor.

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10. The process of forming a capacitor-less memory cell of claim 9, wherein the etching further comprises retaining a stem portion of the bulk semiconductor substrate to physically integrally connect the active area with the bulk semiconductor substrate.

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11. The process of forming a capacitor-less memory cell of claim 10, wherein forming the pass transistor further comprises forming at least a portion of the gate of the read/write enable transistor along at least one side of the stem portion.

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12. The process of forming a capacitor-less memory cell of claim 11, further comprising forming oxide isolation on at least another side of the stem portion between the active area and the bulk semiconductor substrate.

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13. The process of forming a capacitor-less memory cell of claim 10, further comprising implanting the source region of the read/write enable transistor prior to etching the active area.

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14. The process of forming a capacitor-less memory cell of claim 13, further comprising locating the source region of the read/write enable transistor in the bulk semiconductor substrate under the stem portion.

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15. The process of forming a capacitor-less memory cell of claim 9, further comprising forming a commonly shared source region of the pass transistor and the drain region of the read/write enable transistor extending substantially through the thickness of the active area.

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16. A memory device, comprising:  
a memory array including a plurality of capacitor-less memory cells, wherein each of  
the plurality of capacitor-less memory cells includes an active area formed  
from a substantially physically isolated portion of a bulk semiconductor  
substrate, a pass transistor formed on the active area, the pass transistor  
5 including a source region, a drain region for coupling with a digit line and a  
gate for coupling with a word line, and a read/write enable transistor  
including a gate, a source region and a drain region commonly shared with  
the source region of the pass transistor, the read/write enable transistor  
10 vertically configured along at least one vertical side of the active area and  
operable during a reading of a logic state, the logic state being storable as  
charge in a floating body area of the active area to cause different  
determinable threshold voltages for the pass transistor; and  
addressing and sensing circuitry coupled to the memory array and configured to  
15 select and read and write to selected ones of the plurality of capacitor-less  
memory cells.

17. The memory device of claim 16, wherein each of the capacitor-less  
memory cells and the sensing circuitry is configured to determine the logic states  
20 based upon the presence or absence of current flow from the capacitor-less memory  
cell.

18. The memory device of claim 17, wherein the current flow from the  
capacitor-less memory cell is responsive to an amount of charge stored in a floating  
25 body area of the active area to cause the different determinable threshold voltages of  
the pass transistor.

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19. A method of writing data to a capacitor-less memory cell,  
comprising:  
storing determinable amounts of charge in a floating body area of an active area  
having a pass transistor formed thereon; and  
5 altering a threshold voltage designating determinable logic states of the pass  
transistor as the charge is stored in the floating body area of the active area.
20. A method of reading data from a capacitor-less memory cell,  
comprising:  
10 activating a read/write enable transistor vertically configured along at least one side  
of an active area; and  
activating a pass transistor coupled between the read/write enable transistor and a  
sense amplifier, the pass transistor having a threshold voltage responsive to  
stored charge in a floating body area of the active area resulting in the  
15 threshold voltage of the pass transistor designating determinable logic states.
21. A semiconductor wafer including an integrated circuit configured as a  
memory device including a memory array, the memory array including a plurality of  
capacitor-less memory cells, wherein each of the plurality of capacitor-less memory  
20 cells includes an active area formed from a substantially physically isolated portion  
of a bulk semiconductor substrate, a pass transistor formed on the active area, the  
pass transistor including a source region, a drain region for coupling with a digit line  
and a gate for coupling with a word line, and a read/write enable transistor including  
a gate, a source region and a drain region commonly shared with the source region of  
25 the pass transistor, the read/write enable transistor vertically configured along at  
least one vertical side of the active area and operable during a reading of a logic  
state, the logic state being storable as charge in a floating body area of the active area  
to cause different determinable threshold voltages for the pass transistor.

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22. An electronic system including an input device, an output device, a memory device, and a processor device coupled to the input, output and memory devices, the memory device comprising a memory array including a plurality of capacitor-less memory cells, wherein each of the plurality of capacitor-less memory cells includes an active area formed from a substantially physically isolated portion of a bulk semiconductor substrate, a pass transistor formed on the active area, the pass transistor including a source region, a drain region for coupling with a digit line and a gate for coupling with a word line, and a read/write enable transistor including a gate, a source region and a drain region commonly shared with the source region of the pass transistor, the read/write enable transistor vertically configured along at least one vertical side of the active area and operable during a reading of a logic state, the logic state being storable as charge in a floating body area of the active area to cause different determinable threshold voltages for the pass transistor.

23. An electronic system including an input device, an output device and a processor device coupled to the input device and output device, the processor device comprising a memory array including a plurality of capacitor-less memory cells, wherein each of the plurality of capacitor-less memory cells includes an active area formed from a substantially physically isolated portion of a bulk semiconductor substrate, a pass transistor formed on the active area, the pass transistor including a source region, a drain region for coupling with a digit line and a gate for coupling with a word line, and a read/write enable transistor including a gate, a source region and a drain commonly shared with the source region of the pass transistor, the read/write enable transistor vertically configured along at least one vertical side of the active area and operable during a reading of a logic state, the logic state being storable as charge in a floating body area of the active area to cause different determinable threshold voltages for the pass transistor.