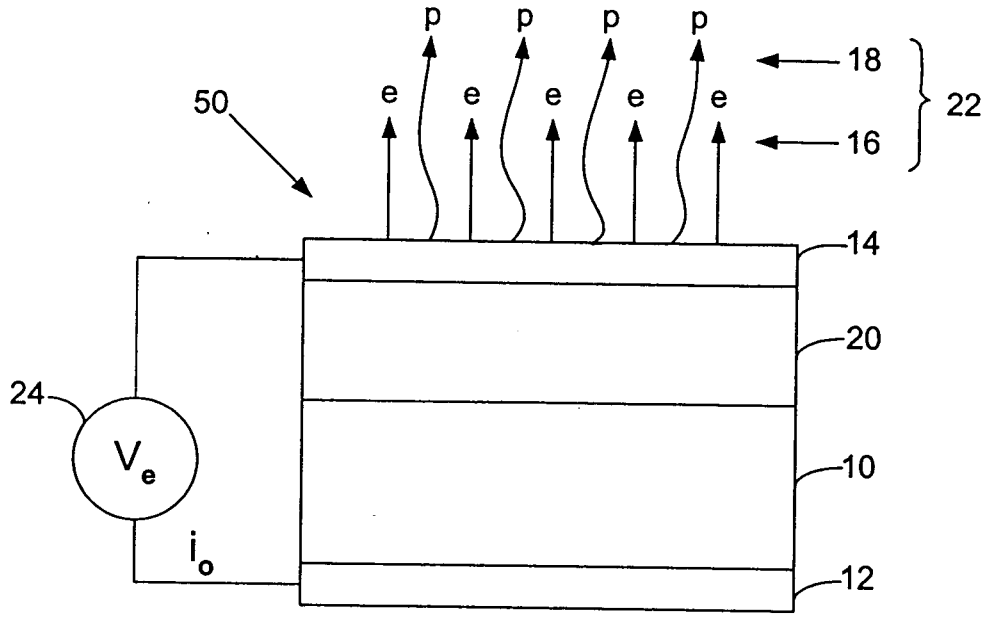

p
p
p
p
e
e
e
e
e
18
16
22
50
14
20
24
V_e
10
i_o
12

Fig. 1

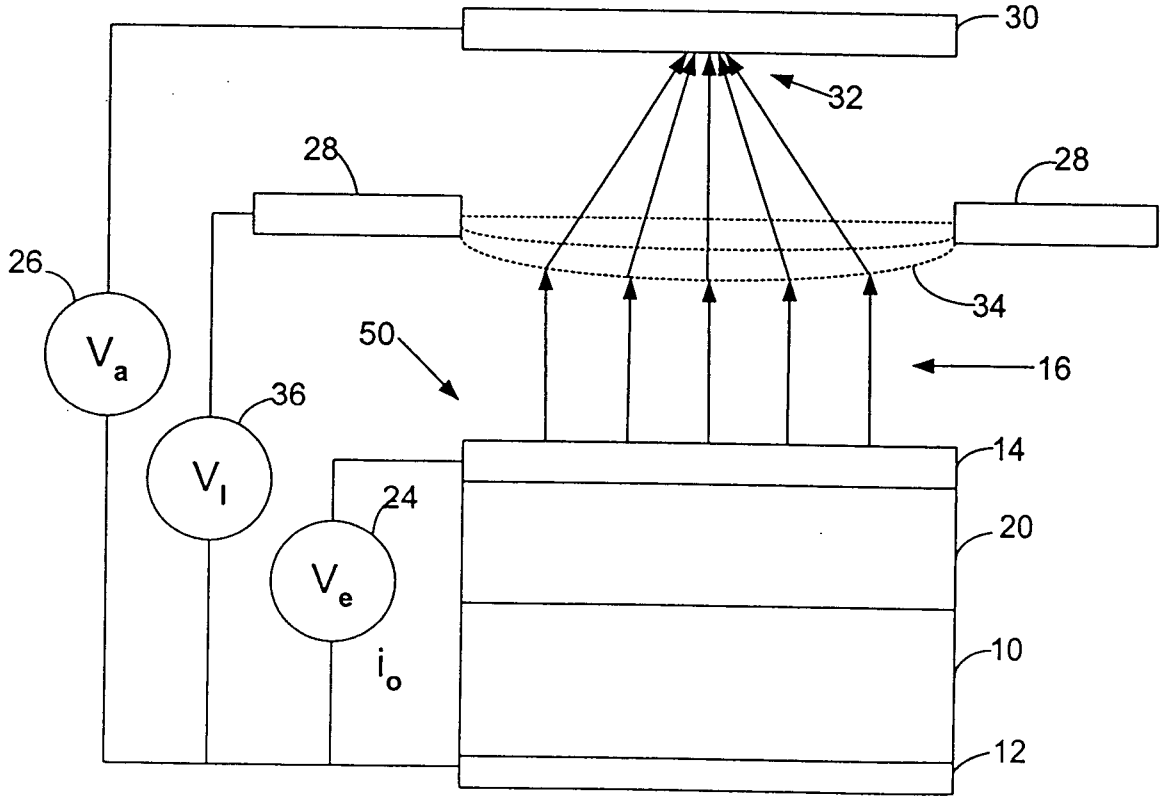

30
32
28
28
26
34
50
16
36
V_a
V_I
24
V_e
14
20
10
i_o
12

Fig. 2

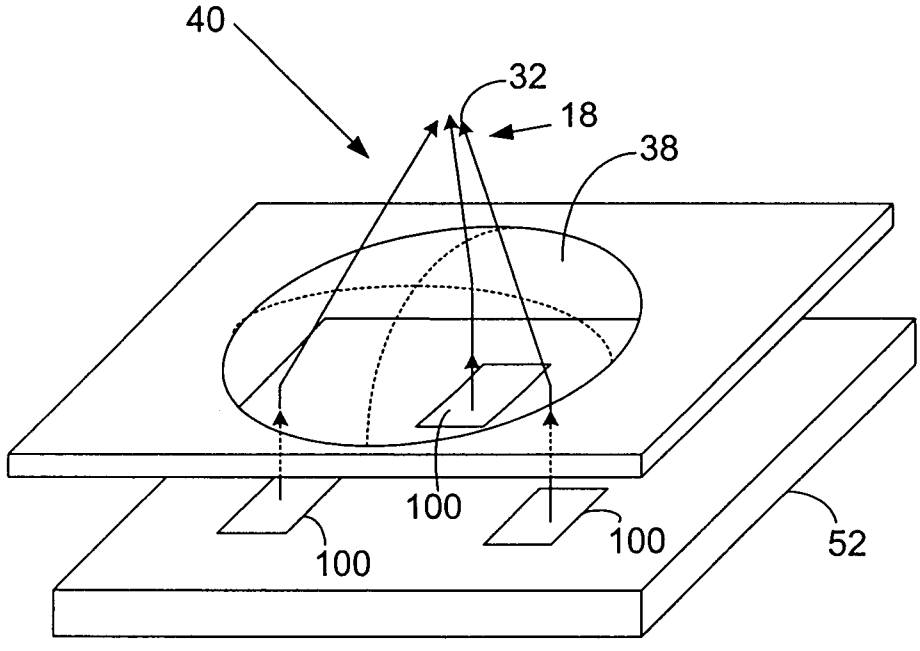


Fig. 3

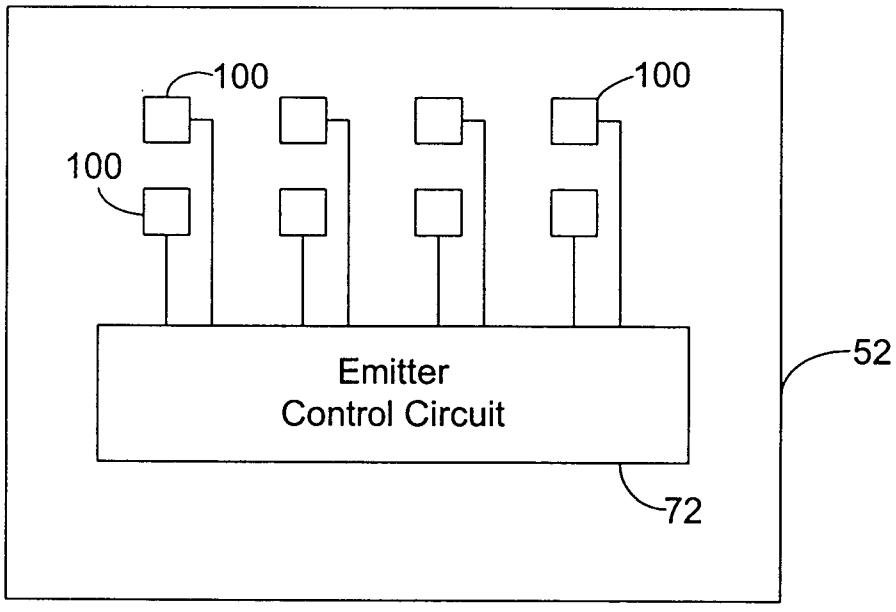

100
100
100
Emitter
Control Circuit
52
72

Fig. 4

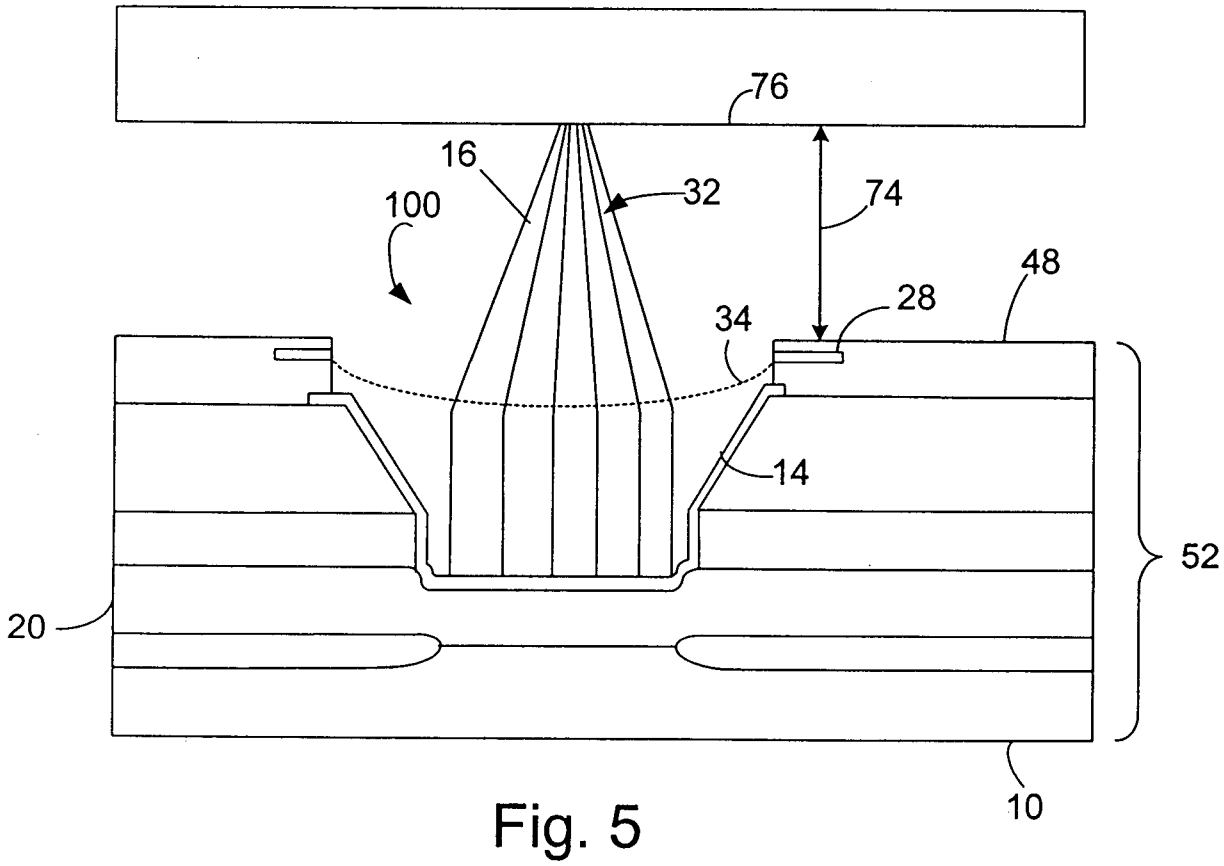

76
16
100
32
74
48
28
34
14
52
20
10

Fig. 5

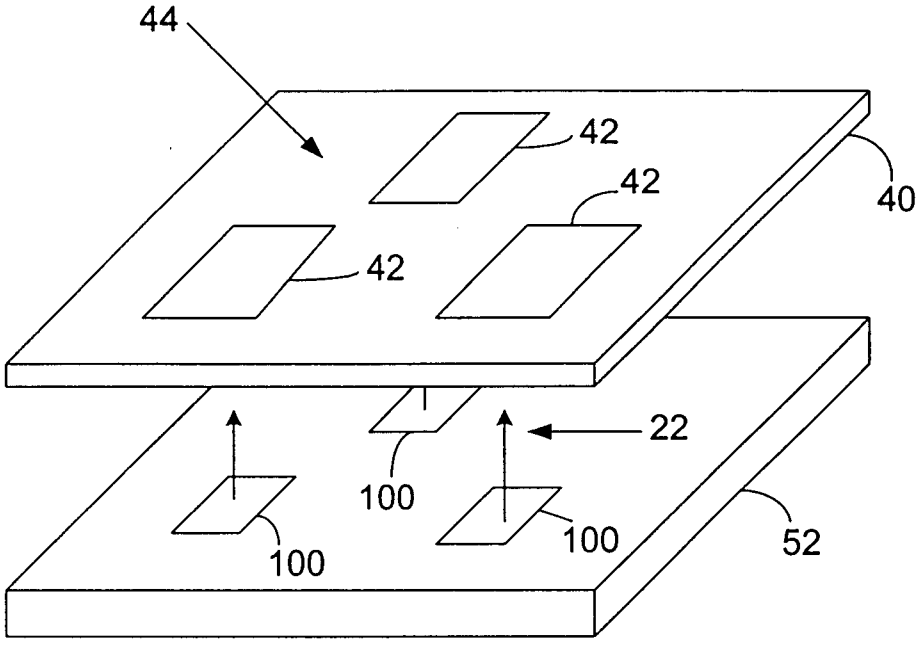

44
42
42
42
40
22
100
100
100
52

Fig. 6

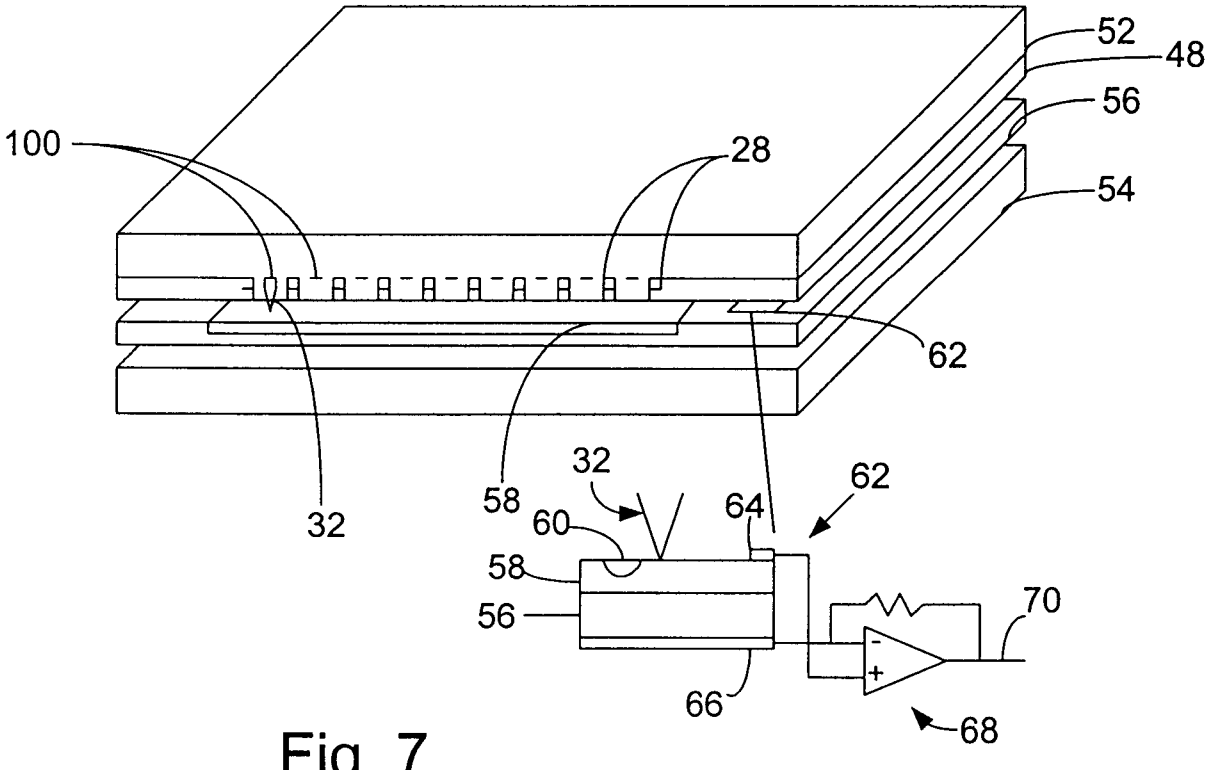

52
48
56
54
100
28
62
32
58
32
60
64
62
58
56
70
66
68

Fig. 7

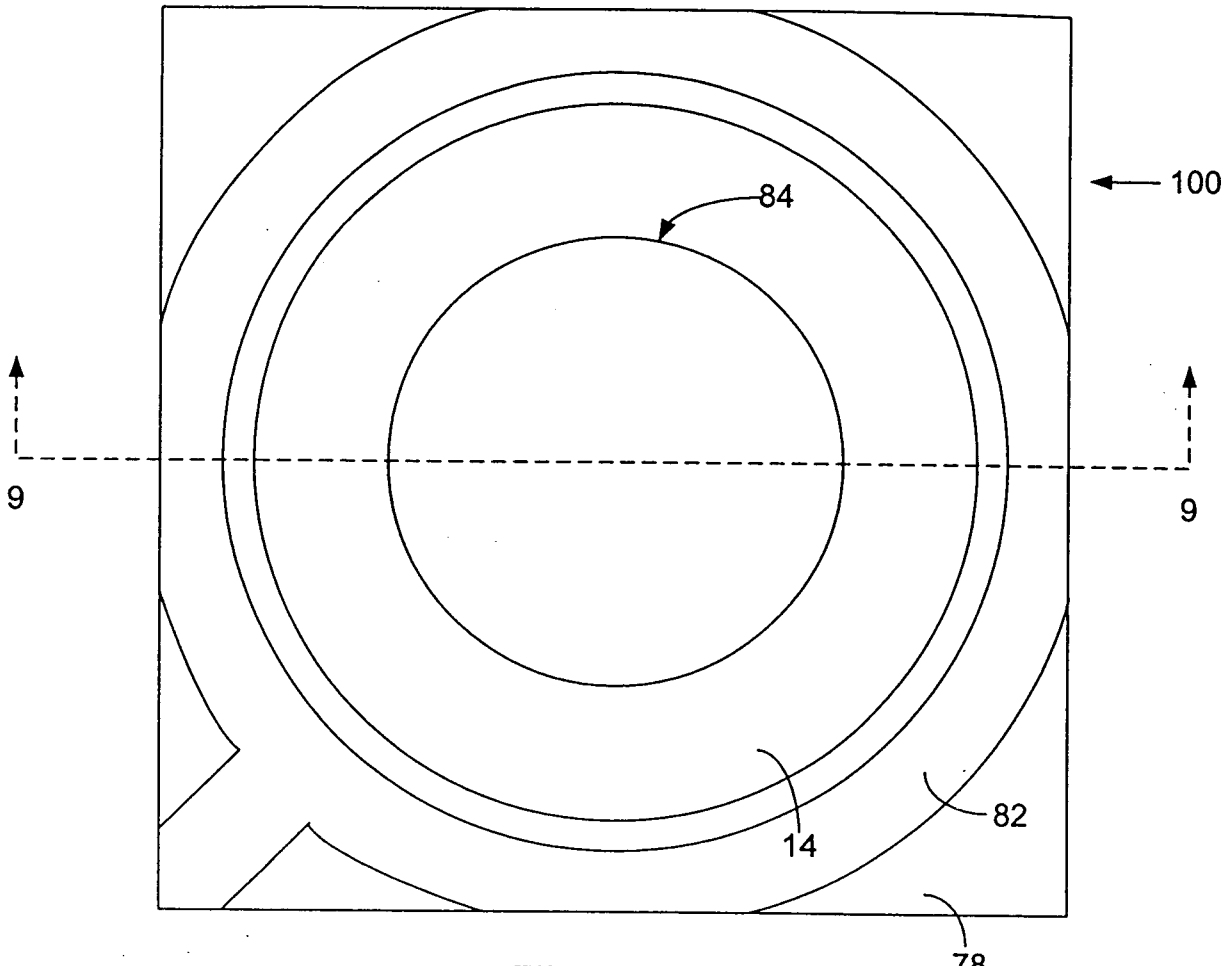


Fig. 8

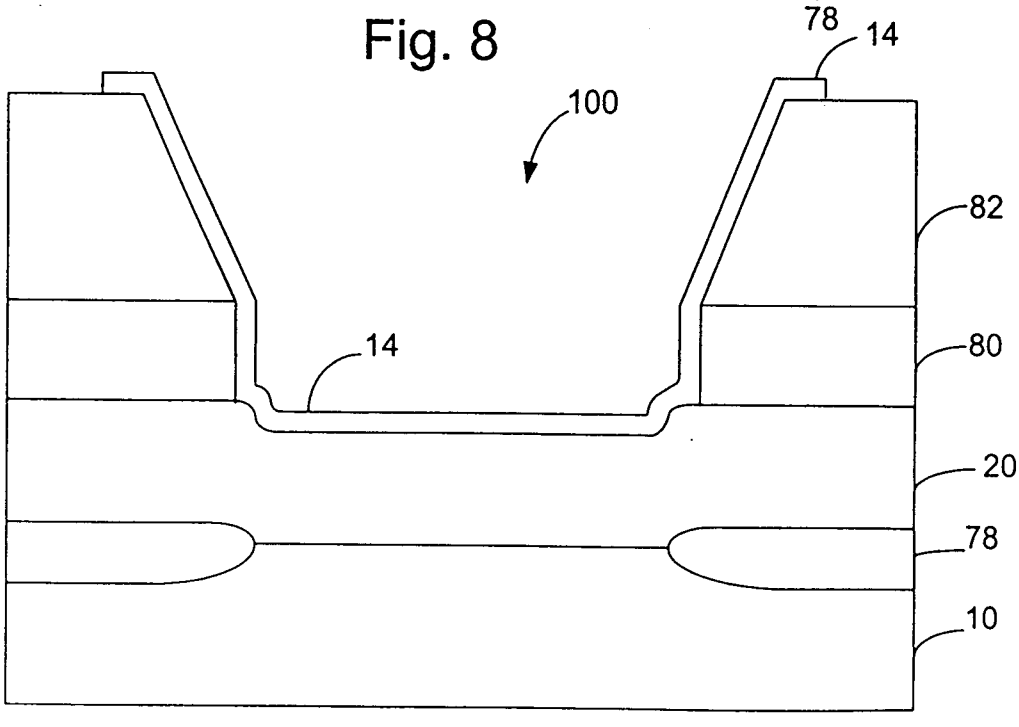


Fig. 9

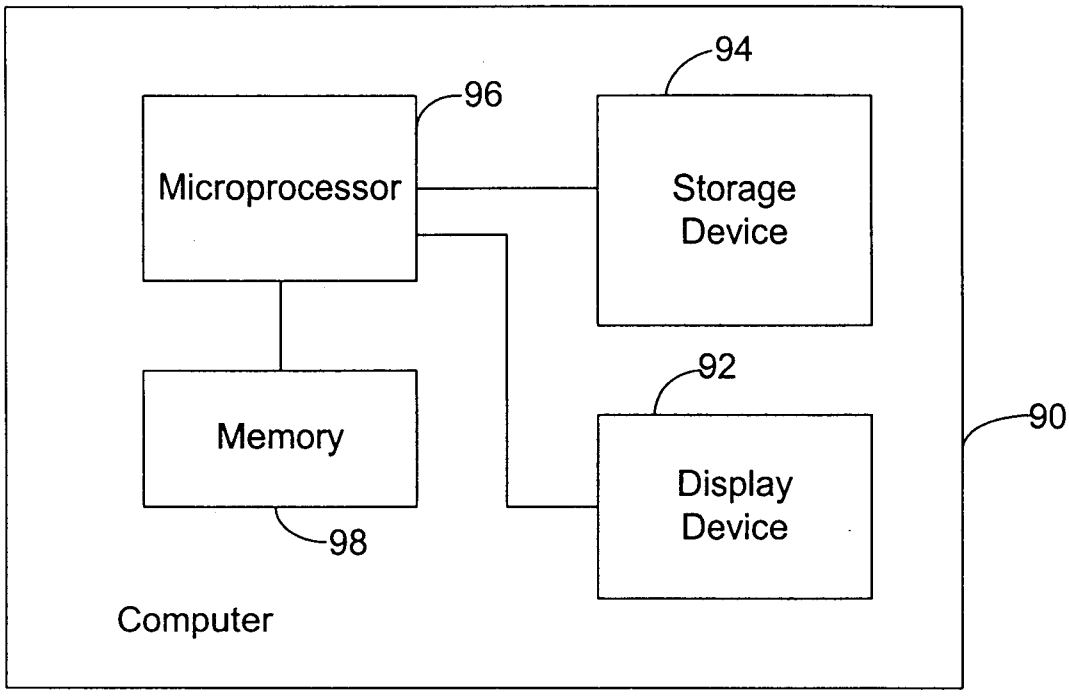

94
96
Microprocessor
Storage Device
92
Memory
Display Device
90
98
Computer

Fig. 10

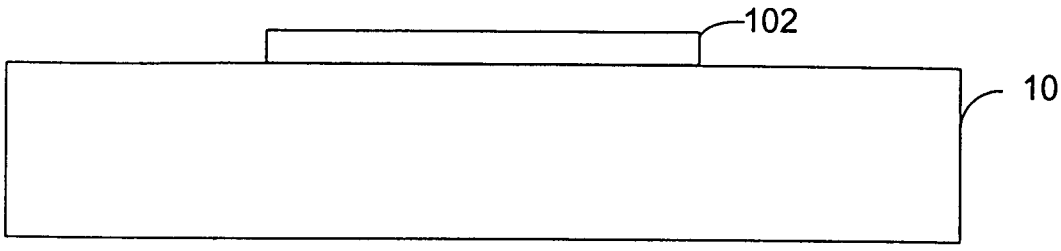


Fig. 11A

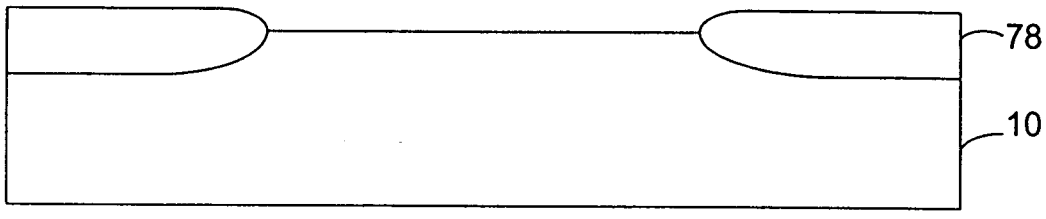


Fig. 11B

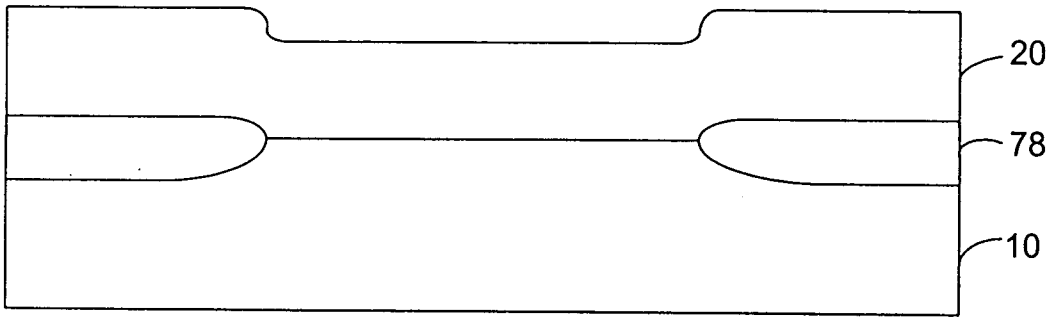


Fig. 11C

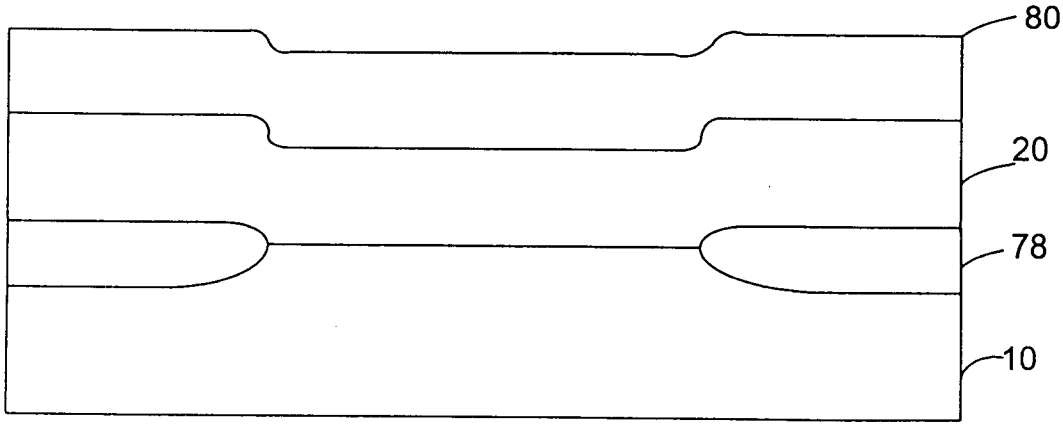


Fig. 11D

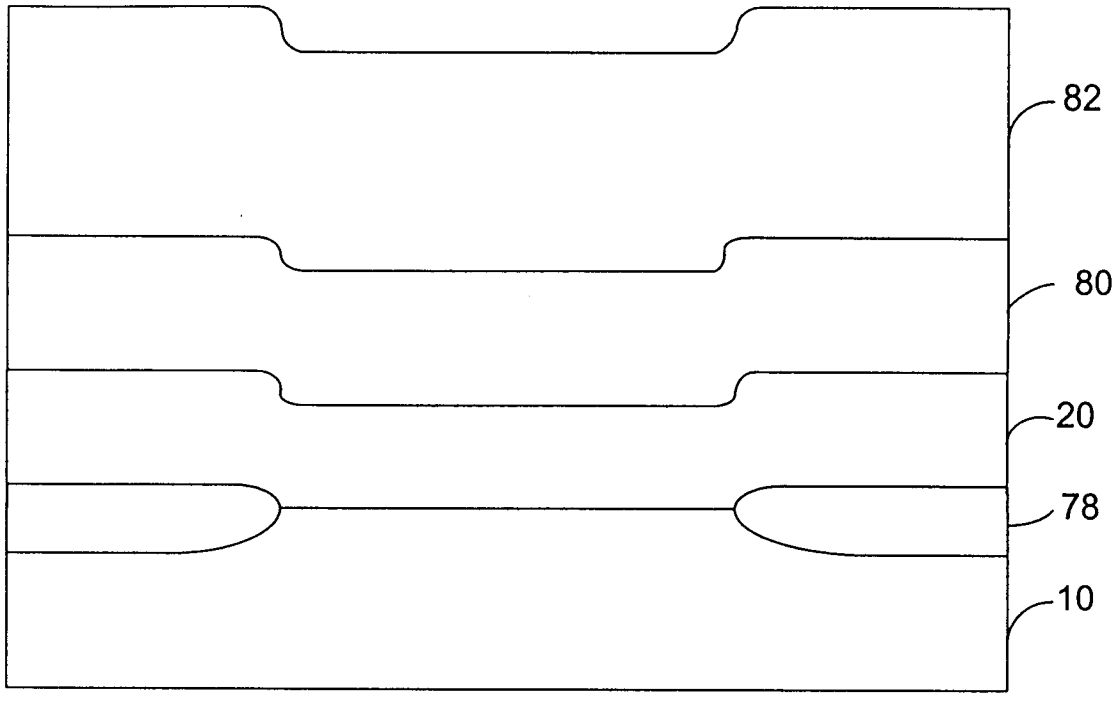


Fig. 11E

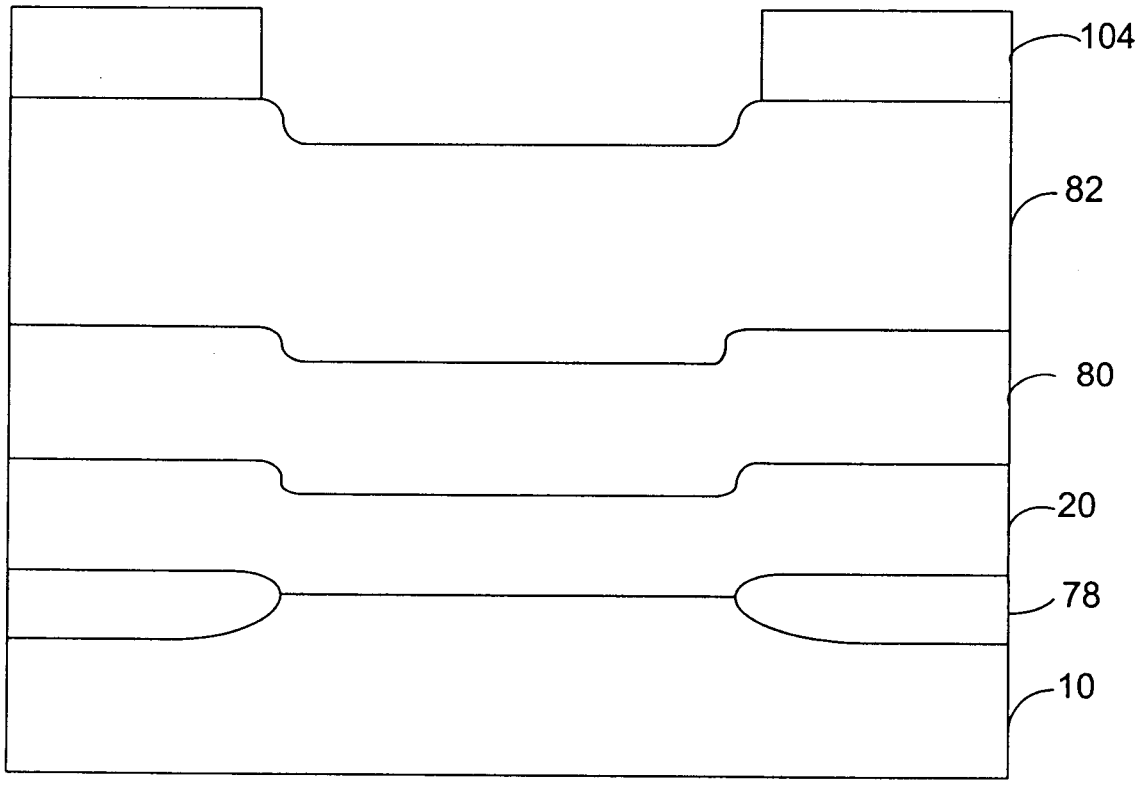


Fig. 11F

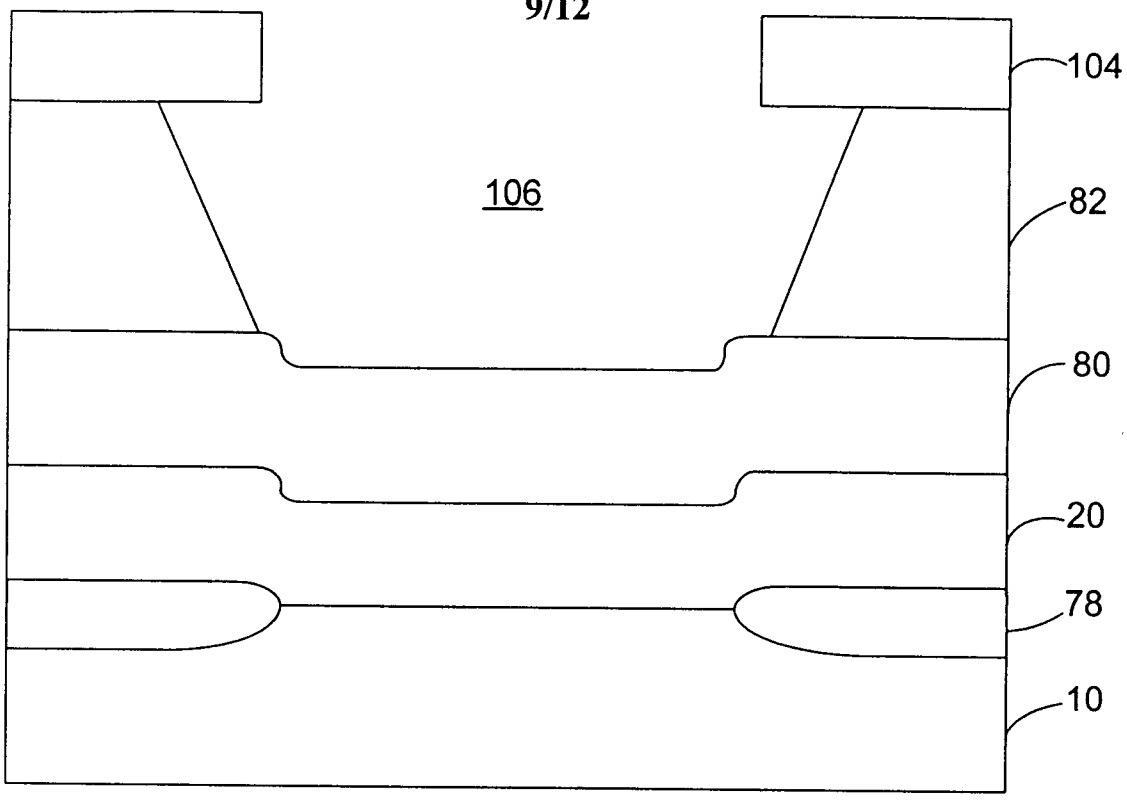


Fig. 11G

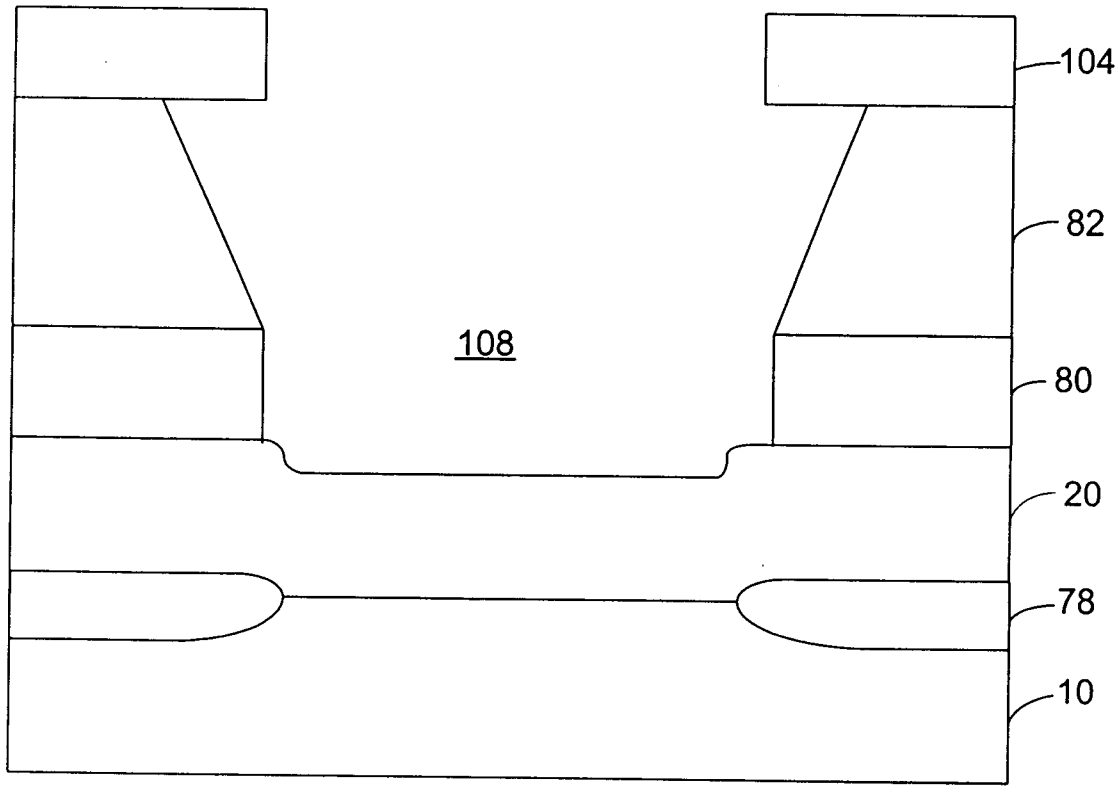


Fig. 11H

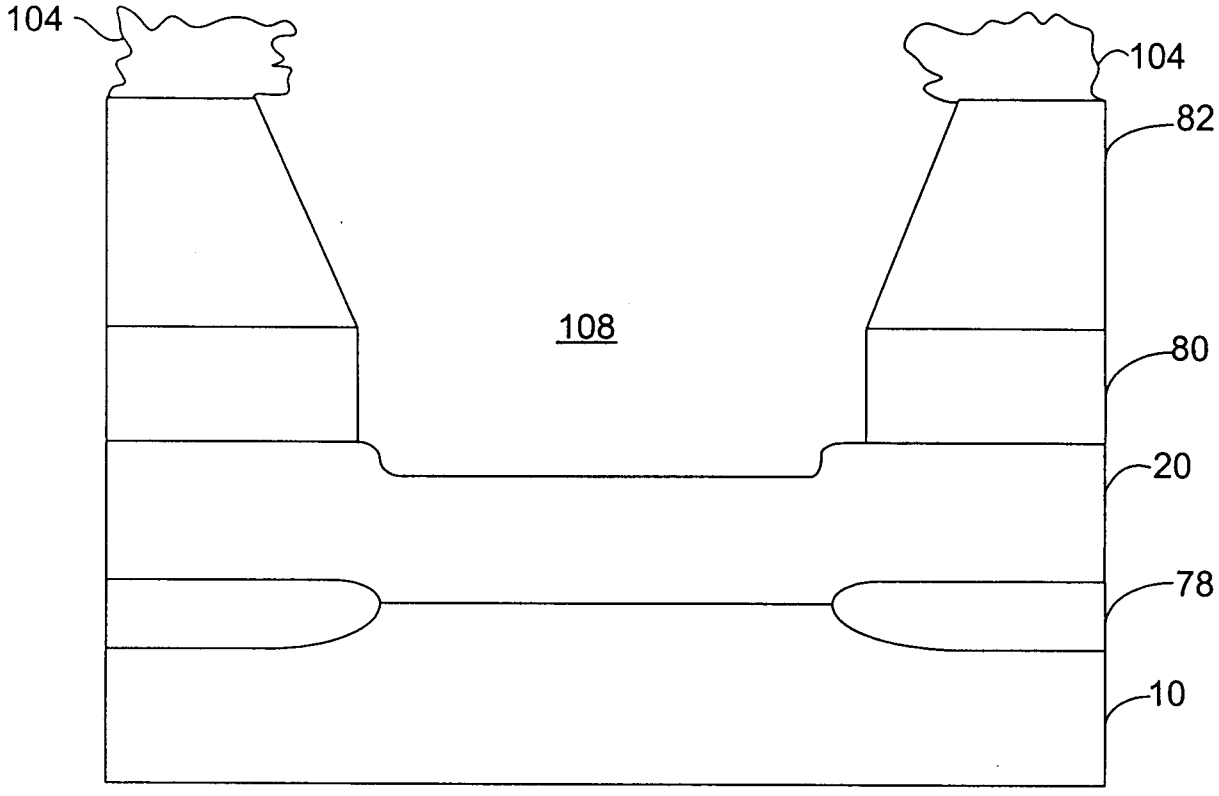


Fig. 11I

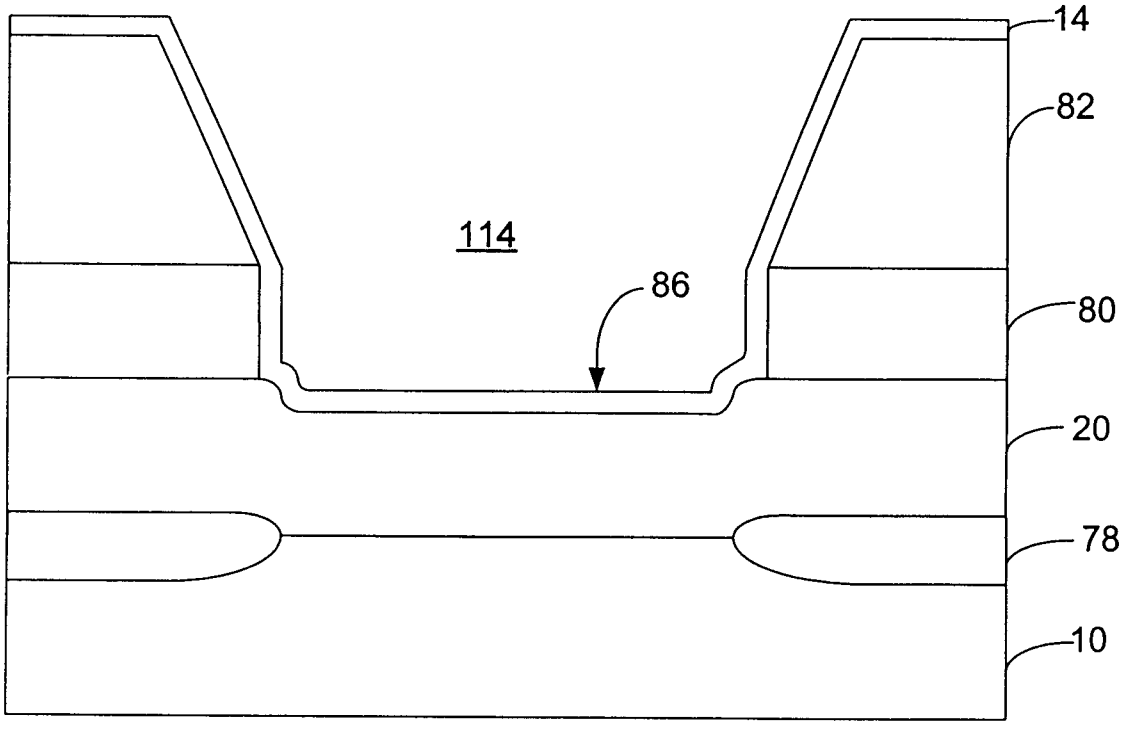


Fig. 11J

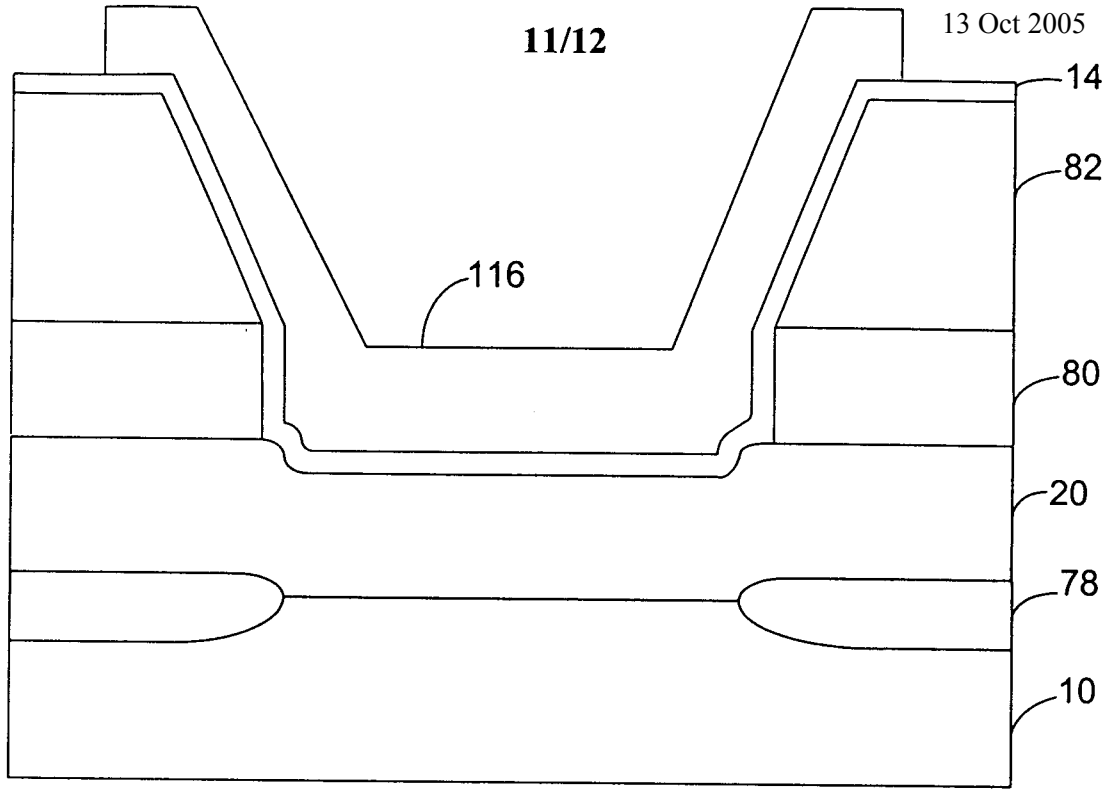


Fig. 11K

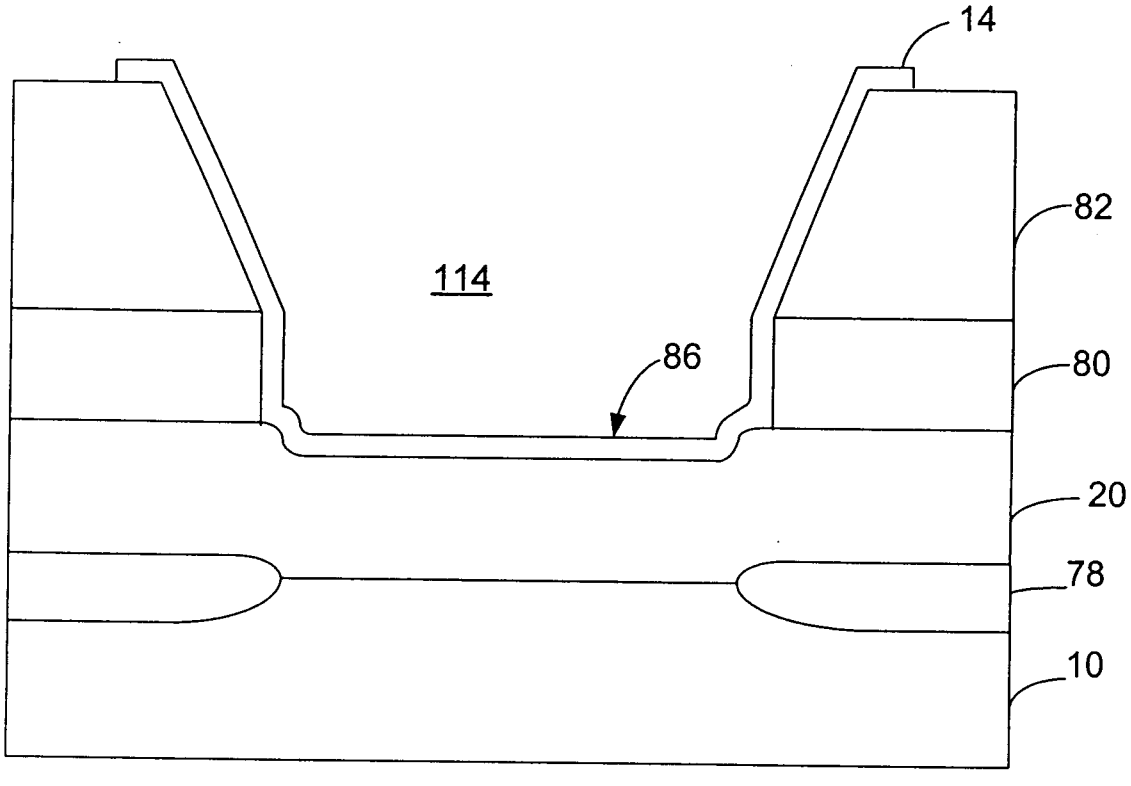


Fig. 11L

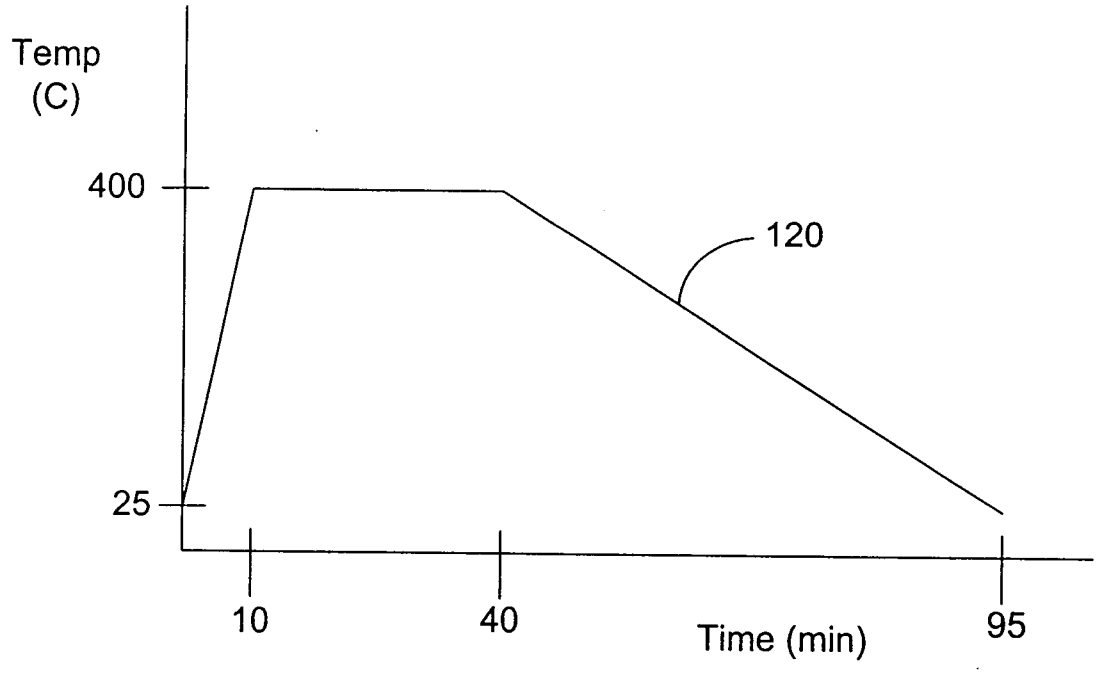


Fig. 12A

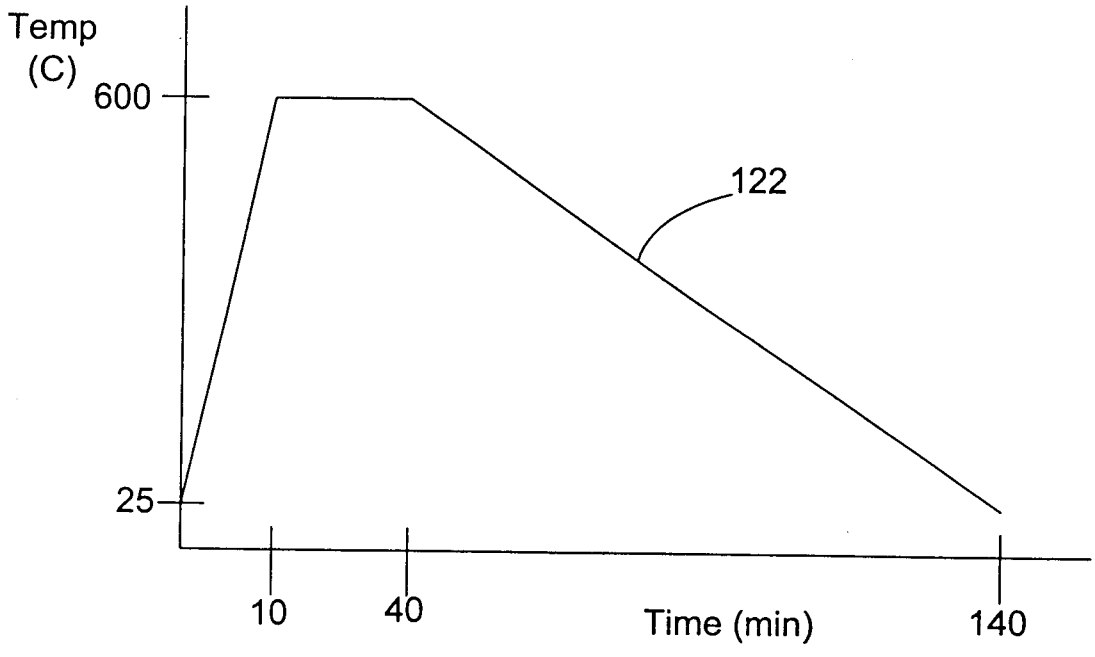


Fig. 12B