

MULTI-JUNCTION SOLAR CELLS

Related Applications

[0001] This application claims priority to and the benefit of U.S. provisional patent application numbers 60/970,808, filed September 7, 2007, and 60/980,103, filed October 15, 2007. The disclosures of both of these applications are incorporated by reference herein in their entireties.

Field of the Invention

[0002] The present invention relates to multi-junction solar cells that convert sunlight to electricity.

Background

[0003] The need for lattice matching, or quasi-lattice matching, is a constraint on efforts to build high-efficiency III-V multi-junction solar cells. Lattice matching in solar cells reduces crystallographic defects that may cause non-radiative recombination of electron-hole pairs. (When pairs recombine before a p-n junction separates them, the efficiency of the solar cell diminishes.) Presently, the need for lattice-matching strongly influences selection of materials for use in solar cells and, as a result, efficiency may be compromised.

Summary

[0004] Embodiments of the present invention allows different materials in a multi-junction solar cell to be selected to increase the cell's performance without being constrained by the need for lattice-matching. Bandgaps and lattice constants of common III-V semiconductors are indicated in Figure 1. Recently it has been demonstrated that solar cells using a substantially lattice-matched indium gallium phosphide / gallium arsenide / germanium (InGaP / GaAs / Ge) configuration (illustrated with dashed lines in Figure 1) formed on Ge substrates achieved the relatively high efficiency of 40.1% in converting sunlight into electricity. A solar cell's energy conversion efficiency (η , "eta") is the percentage of power converted (from absorbed light to electrical energy) and collected, when a solar cell is connected to an electrical circuit. This value may be calculated using a ratio of a maximum power point, P_m , to the input light

irradiance (E , in W/m^2) under standard test conditions (STC) and the surface area of the solar cell according to the following equation (A_c in m^2).

$$\eta = \frac{P_m}{E \times A_c}$$

5 [0005] STC are typically a temperature of 25°C and an irradiance of $1000 \text{ W}/\text{m}^2$ with an air mass of 1.5 (AM1.5) spectrum.

[0006] A three-junction solar cell tailored to increase efficiency without regard for lattice matching, however, may employ a configuration other than the aforementioned InGaP / GaAs / Ge configuration, because the bandgaps (shown in Table 1 below) of the lattice-matched
10 materials offer a sub-optimal way of capturing the solar spectrum. In particular, the theoretical efficiency of a solar cell reaches its maximum when it absorbs each portion of the sun's spectrum with a material that has a bandgap close to the photon energy of the respective portion of the sun's spectrum. In the example of Figure 1, the 1.42 eV bandgap of GaAs is far from the bandgap of approximately 1.1 eV that was determined by modeling to be more suitable as the
15 middle material in a three-junction cell with InGaP and Ge. The modeling included making a mathematical model of each sub-cell in which the bandgap is one of the variables, setting the currents equal to each other, and running an efficiency optimization algorithm varying each bandgap.

[0007] The different photovoltaic cells that make up a multi-junction cell may be referred to
20 herein as "sub-cells," Including photovoltaic sub-cells or solar sub-cells. Thus, a sub-cell is a fully functional photovoltaic cell, and multiple sub-cells are included in the devices described herein. The preferred bandgap of the materials of a sub-cell in a multi-junction solar cell is determined by several factors. If the bandgap in a sub-cell is too high, then photons with an energy below the bandgap may pass through the sub-cell without being absorbed, and the
25 energy of that photon may be lost unless it is absorbed by a lower cell. If the bandgap of a sub-cell is too low, then more photons may be absorbed by that sub-cell, but the higher energy photons may be absorbed inefficiently. A preferred bandgap energy represents a compromise between these two effects.

Table 1 - Bandgaps of $\text{In}_{0.5}\text{Ga}_{0.5}\text{P}$, GaAs, and Ge

Material	Bandgap (eV)
$\text{In}_{0.5}\text{Ga}_{0.5}\text{P}$	1.86
GaAs	1.42
Ge	0.66

[0008] Figure 2 shows several possible combinations of materials for a three-junction solar cell with bandgaps that provide a theoretical ability to convert solar energy to electricity with 63.2% efficiency.

5 **[0009]** As discussed in detail below, embodiments that use silicon (Si) as a middle sub-cell in a multi-junction solar cell provide improved performance and reduced cost. Various embodiments described herein use Si in solar cell configurations that utilize Si substrates and modern Si processing. In some embodiments, aspect ratio trapping (ART) techniques provide an effective mechanism for depositing high-quality non-lattice-matched materials on Si. *See,*
 10 *e.g.*, U.S. Patent Publication No. 2006/0292719, incorporated by reference herein.

[0010] While Ge is currently the substrate of choice in III-V solar cells because of the lattice match of Ge with GaAs, two practical issues are associated with the use of Ge as a substrate. First, Ge substrates contribute to the high cost of III-V solar cells: they are smaller and more expensive than Si substrates, and they rule out modern Si processing as a cost-reduction
 15 technique. Also, the limited supply of Ge substrates may restrict growth of the market for these devices.

[0011] Two key technical barriers hinder the integration of III-V solar cells onto a Si platform: the mismatch of lattice constants and the mismatch of thermal expansion coefficients. In particular, when a material with a lattice constant greater than that of Si is
 20 grown on Si, its atoms experience compressive strain because they adopt the shorter interatomic distances of the Si template. Below a critical thickness t_c (typically several atomic layers for materials with substantial mismatch), the epitaxial layer remains “pseudomorphic” or “fully strained.” Above t_c , the epitaxial layer relaxes, i.e., it assumes its normal lattice parameters to relieve the strain. Misfit dislocations appear at – and propagate along – the
 25 interface between the substrate and the epitaxial layer.

[0012] Misfit dislocations terminate at the edge of a crystal or at a threading dislocation, i.e., a defect that propagates upward from the interface. In cubic lattices, threading dislocations lie along $\langle 110 \rangle$ crystal directions; they typically approach the surface at a 45° angle to the substrate. Threading dislocations may degrade device performance and reliability. In solar cells, they may promote recombination of electrons and holes, thereby reducing efficiency. The threading dislocation density (TDD) in III-V materials grown directly on Si is typically approximately $10^9 / \text{cm}^2$.

[0013] Thermal expansion mismatch may lead to processing difficulties. Growth temperatures of III-V films typically range from 450°C to 800°C . When a Si substrate cools, the III-V material disposed thereover may contract more than the Si. The substrate may bow in a concave manner, stressing and ultimately cracking the film.

[0014] Previous efforts to integrate non-Si semiconductors onto Si substrates have relied primarily on three approaches: graded buffer layers, wafer bonding, or selective epitaxy on mesa regions. Each of these approaches has demonstrated significant limitations, as described below.

[0015] Graded buffer layers provide a gradual change in lattice constant from the silicon substrate to the active region of the epitaxial material. However, the typical thickness of the graded buffer layer (10 micrometers (μm) of epitaxial growth for a 4% lattice-mismatch) increases the expense of epitaxy and exacerbates cracking.

[0016] Wafer bonding involves growing devices on lattice-matched substrates, then lifting off the devices and bonding them to a Si substrate. This approach is relatively costly and may be incompatible with modern Si processing. Furthermore, the difference between the thermal expansion coefficients of the bonded materials and the Si may lead to cracking.

[0017] Selective epitaxy on mesa regions is a technique that attempts to exploit the glissile behavior of some dislocations. The strategy includes depositing III-V materials in mesa regions 10 to $100 \mu\text{m}$ in length, thereby providing a short path along which threading dislocations may glide to the edge of the region and remove themselves from the device. However, structures created by selective epitaxy on mesa regions typically have a high TDD, above $10^8 / \text{cm}^2$, perhaps because selective epitaxy may not remove sessile (immobile) dislocations, which dominate when the lattice-mismatch exceeds 2%.

[0018] While some embodiments of the invention may include elements of the foregoing approaches, other embodiments take advantage of the ART approach to integrate non-Si semiconductors onto Si substrates.

[0019] In an aspect, embodiments of the invention feature a structure including a

5 semiconductor substrate having a top surface and a bottom surface. A top insulator layer is disposed proximate the top surface of the substrate and defines a top opening. A bottom insulator layer is disposed proximate the bottom surface of the substrate and defines a bottom opening. A first crystalline layer is disposed within the top opening, the first crystalline layer being lattice-mismatched to the semiconductor substrate, with a majority of lattice-mismatch
10 defects that arise at a surface of the first crystalline layer nearest the substrate terminating within the top opening. A second crystalline layer is disposed within the bottom opening. The second crystalline layer being lattice-mismatched to the semiconductor substrate, and a majority of lattice-mismatch defects arising at a surface of the second crystalline layer nearest the substrate terminate within the bottom opening.

15 [0020] In another aspect, an embodiment of the invention features a structure including a substrate, and a first photovoltaic sub-cell formed above the substrate, including a first semiconductor material having a first lattice constant. A second photovoltaic sub-cell is formed below the first sub-cell, and includes a second semiconductor material having a second lattice constant different from the first lattice constant. A third photovoltaic sub-cell is formed
20 below the second photovoltaic cell and below the substrate, and includes a third semiconductor material having a third lattice constant different from the second lattice constant.

[0021] In some embodiments, the first semiconductor material includes or consists essentially of a III-V compound, and the first photovoltaic sub-cell comprises a first photovoltaic junction defined by the III-V compound. The second photovoltaic sub-cell may
25 include a second photovoltaic junction defined in the substrate. In a particular embodiment, the first photovoltaic sub-cell includes a first III-V compound, the second photovoltaic sub-cell includes or consists essentially of silicon, and the third photovoltaic cell includes a second III-V compound. In various embodiments, the substrate includes silicon. A compositionally graded buffer layer may be disposed between the first and second photovoltaic sub-cells. A
30 defect-trapping layer may be disposed between the first and second photovoltaic sub-cells, the defect-trapping layer including (i) a crystalline material comprising defects arising from lattice-

mismatch of the crystalline material with an adjacent semiconductor material and (ii) a non-crystalline material, the defects terminating at the non-crystalline material.

[0022] In still another aspect, an embodiment of the invention includes a structure comprising includes a first photovoltaic sub-cell including a first semiconductor material having a first lattice constant and a first bandgap energy. A second photovoltaic sub-cell includes a second semiconductor material having a second lattice constant different from the first lattice constant and a second bandgap energy lower than the first bandgap energy. A defect-trapping layer is disposed between the first and second photovoltaic sub-cells, and has a third bandgap energy higher than the second bandgap energy. The defect-trapping layer includes a crystalline material proximate and in contact with a non-crystalline material, the crystalline material including defects terminating at the non-crystalline material.

[0023] In another aspect, embodiments of the invention include a structure featuring a first defect-trapping layer that includes a first crystalline material proximate and in contact with a first non-crystalline material, with the first crystalline material including defects arising from a lattice-mismatch of the first crystalline material to a first adjacent material, the defects terminating at the first non-crystalline material. A second defect-trapping layer is disposed below the first defect-trapping layer. The second defect-trapping layer includes a second crystalline material proximate and in contact with a second non-crystalline material. The second crystalline material includes defects arising from a lattice-mismatch to a second adjacent material, the defects terminating at the second non-crystalline material.

[0024] The first and second defect-trapping layers may be disposed on opposite sides of a substrate, the substrate includes the first and second adjacent materials, which may be the same material. The first and second defect-trapping layers may each be disposed above a substrate, which includes the first adjacent material, and the first crystalline material includes the second adjacent material. A solar cell is disposed between the first and second defect-trapping layers, below the second defect-trapping layer, or above the first defect-trapping layer. A first semiconductor layer having a first lattice constant is disposed above the first defect-trapping layer, and a second semiconductor layer having a second lattice constant different from the first lattice constant is disposed above the second defect-trapping layer.

[0025] In still another aspect, the invention includes a method of forming a photonic device. The method includes providing a substrate. A first active photonic device layer above the substrate, and a second active photonic device layer is formed below the substrate. Forming each of the first and second active photonic device layers includes epitaxial growth. The substrate may include a third photonic device layer. The first active photonic device layer may include a first solar cell junction and the second active photonic device layer may include a second solar cell junction.

[0026] In another aspect, an embodiment of the invention features a multi-junction solar cell device. The device includes a first solar cell including a first non-Si photovoltaic junction, a second solar cell disposed below the first solar cell and including a Si photovoltaic junction, and a third solar cell disposed below the second solar cell and second a second non-Si photovoltaic junction.

[0027] In yet another aspect, embodiments of the invention feature a multi-junction solar cell device. The device includes a first solar sub-cell having a first energy bandgap. It also includes a second solar sub-cell formed below the first solar sub-cell and having a second energy bandgap greater than the first energy bandgap and approximately equal to 1.1 eV. A third solar sub-cell is formed below the second solar cell and has a third energy bandgap greater than the second energy bandgap. The first energy bandgap may be less than 1.1 eV, and preferably less than about 0.8 eV, and the third energy bandgap may be greater than 1.1 eV. The second bandgap is generally selected from a range of about 1.0 eV to about 1.2 eV. The third energy bandgap is generally greater than about 1.6 eV.

Brief description of the drawings

[0028] Figure 1 is a graph illustrating the bandgaps and lattice constants of common lattice-matched III-V semiconductor materials;

Figure 2 is a graph illustrating selection of materials for a non-lattice-matched three-junction solar cell with bandgaps that provide a theoretical ability to convert solar energy to electricity with 63.2% efficiency;

Figure 3 is a schematic diagram illustrating the basic principles of ART;

Figure 4 and 5 are schematic diagrams illustrating facet formation adjacent a dielectric sidewall;

Figure 6 is a schematic diagram illustrating growth planes of a material formed by
5 employing ART;

Figures 7 - 10 are schematic diagrams illustrating various samples formed by employing ART;

Figure 11 is a schematic diagram illustrating a three-junction solar-cell structure;

Figure 12 is a schematic diagram illustrating an ART structure for growing InGaP;

10 Figure 13 is a schematic diagram illustrating various growth modes of lattice-mismatched materials;

Figure 14 is a schematic diagram illustrating growth of wide bandgap InP below InGaAs in an ART region;

15 Figure 15 is a schematic diagram illustrating a structure for a single-junction InGaP solar cell;

Figure 16 is a schematic diagram illustrating an architecture for a single junction InGaAs solar cell;

Figure 17 is a schematic diagram illustrating a dual-junction InGaP/Si solar cell;

Figure 18 is a schematic diagram illustrating a dual-junction InGaAs/Si solar cell;

20 Figure 19 is a schematic diagram illustrating an alternative architecture for a single junction InGaAs solar cell utilizing a coalesced material;

Figure 20 is a schematic diagram illustrating an alternative embodiment of a InGaP / Si / InGaAs cell with a coalesced buffer region;

25 Figures 21a -21j are a series of schematic diagrams illustrating the fabrication of a three-junction InGaP / Si / InGaAs solar cell;

Figure 22 is a schematic diagram illustrating a five-junction InGaP / GaAs / Si / GaAsSb /InGaAs solar cell;

Figure 23 is a schematic diagram illustrating a three-junction InGaP / GaAs /InGaAs solar cell disposed over a Si substrate;

Figure 24 is a schematic diagram illustrating a three-junction InGaP / Si / InGaAs solar cell incorporating InGaP graded buffer layers on both sides of a Si substrate;

5 Figures 25a–25b are schematic diagrams illustrating the use of wafer bonding or layer transfer to create a three-junction InGaP / Si Ge solar cell; and

Figures 26a – 26f are a series of schematic diagrams illustrating an alternative method for forming an ART structure.

Detailed Description

10 **[0029]** As used herein, the terms “solar cell,” “photovoltaic cell,” and “photovoltaic sub-cell” each denote a structure having a photovoltaic junction, e.g., a p-n junction. A “photonic device layer” refers to a photoactive device, such as a solar cell.

[0030] ART enables solar-cell designers to select junction materials on the basis of their bandgaps without being constrained by their lattice constants. It also enables solar cell
15 manufacturers to take advantage of inexpensive Si substrates and modern Si processing technologies. Multi-junction solar cells fabricated on Si substrates by ART also offer good mechanical strength, light weight, and superior heat dissipation in comparison to Ge substrates. The superior heat dissipation may be especially important in concentrator applications, since solar cells generally work less efficiently at elevated temperatures.

20 **[0031]** ART substantially eliminates problems from threading dislocations arising from a mismatch between the lattice constants of a film and an underlying substrate. It reduces stress due to the mismatch in thermal expansion coefficients, employs standard equipment, and does not require prohibitively expensive processes.

[0032] Referring to Figure 3, an ART structure may be formed in accordance with the
25 following steps. A semiconductor substrate 300, i.e., a semiconductor wafer, is provided. The semiconductor substrate 300 may include a semiconductor material and may be, for example, a bulk silicon wafer, or a bulk germanium wafer. The substrate 300 may include or consist essentially of a first semiconductor material, such as a group IV element, e.g., germanium or silicon. In an embodiment, the substrate 100 includes or consists essentially of (300) silicon.

[0033] A dielectric layer 310, including a dielectric material, i.e., a non-crystalline material such as SiO_2 is formed over the semiconductor substrate 300. SiO_2 is just one example of a dielectric material, and those of skill in the art may substitute other materials, such as SiN_x , as appropriate, for example, to reduce recombination effects. The dielectric layer 310 may be formed by a method known to one of skill in the art, e.g., thermal oxidation or plasma-enhanced chemical vapor deposition (PECVD) in a suitable system, such as the CENTURA ULTIMA manufactured by Applied Materials, based in Santa Clara, CA. The dielectric layer may have a thickness t_1 corresponding to a desired height of crystalline material to be deposited in an opening formed through the dielectric layer. In some embodiments, the thickness t_1 of the dielectric layer 310 may range from, e.g., 25 nm to 20 μm .

[0034] A plurality of narrow, sub-micron-width openings, e.g., trenches 320, are defined in the dielectric layer 310 by conventional lithography and reactive ion etching, with the openings having dielectric sidewalls 325. Those of skill also understand how to perform additional steps to adapt the process for various applications, such as treating SiO_2 with a hydrogen plasma to passivate the sidewalls of the trench.

[0035] After cleaning, a lattice-mismatched material 330 is selectively grown within the opening 320. The lattice-matched material may be, e.g., a III-V semiconductor or Ge, grown in the opening by, e.g., selective epitaxy. The threading dislocations in the lattice-mismatched material typically slope towards the sidewalls of the opening and terminate when they reach the dielectric material, e.g., SiO_2 . Accordingly, a region of the epitaxial material near the top of the trench is preferably substantially free of dislocations.

[0036] An ART structure may be used as a defect-trapping layer in the solar cells discussed below. The ART structure includes (i) a crystalline material including defects arising from lattice-mismatch of the crystalline material with an adjacent semiconductor material and (ii) a non-crystalline material, with the defects terminating at the non-crystalline material.

[0037] When depositing a material such as Ge into a trench between SiO_2 sidewalls, the bond between a germanium atom and an oxygen atom requires higher energy than the bond between two Ge atoms. The Ge-O bond is therefore less favorable, and, accordingly, is less likely to form. Accordingly, under typical growth conditions, the Ge atoms form a facet 400, typically a {111} or {113} crystal plane, as shown in Figure 4.

[0038] Between two dielectric sidewalls, two crystal planes, e.g., {111} plane 500, and {100} plane 500' may grow simultaneously. The growth rate of the two planes may be different. For example, in Ge the {100} plane grows faster than the {111} plane, as shown in Figure 5. Eventually the fast growth plane disappears because the crystal growth in the direction of the fast plane is limited by the growth rate of the slow growth plane, as also shown in Figure 5.

[0039] To enable the observation of these two crystalline orientations, thin regions of a marker material defining a marker layer 600 may be interposed within the lattice-mismatched material 330. For example, thin Si-Ge regions, or "marker layers," may be interposed within a Ge matrix to provide contrast in TEM images. These marker layers 600 appear as black chevrons in the schematic representation of a TEM micrograph in Figure 6. The Ge grows with a {100} crystal orientation in the lowest sector of the figure (below the letter A). Above that region, the angled black Si-Ge marker layers show that the Ge has transitioned to {111} growth planes or facets. The following behavior of a threading dislocation 610 is observed:

- It rises vertically from the substrate 300 through the region with the {100} crystal orientation 500', toward the letter A.
- At point A, the threading dislocation intersects the region with the {111} crystal orientation 500. The facets of the crystal direct the threading dislocation to a direction normal to the {111} facet, toward the sidewall.
- The threading dislocation reaches the SiO₂ sidewall and terminates.

[0040] When the threading dislocation reaches a facet boundary, the crystal boundary typically redirects it in a direction perpendicular to the facet. The facet inclines the threading dislocation towards the sidewalls. All threading dislocations in a material having facets non-parallel to an underlying substrate, therefore, typically intersect a sidewall, if the sidewall is sufficiently high. In some embodiments, the aspect ratio of the trench, i.e., the ratio of its height to its width, is preferably greater than about 1. The sidewalls preferably trap the dislocations, leaving a defect-free region of epitaxial material at the top of the trench. This approach substantially eliminates substrate interface defects in one lithography and one selective epitaxial growth step.

[0041] ART samples were prepared with Ge and GaAs. Ge was deposited on Si substrates within SiO₂ trenches. Thin TEM images of samples indicated that the SiO₂ sidewalls trapped all threading dislocations, leaving defect-free Ge at the top of the trenches. Referring to Figure 7, a schematic diagram of a TEM image illustrates that Ge deposited in openings 320, e.g., trenches 200 nm wide, may be free of defects 610 above a trapping region. Top-view (“plan-view”) TEM images of the material were then captured. Figure 8, a schematic diagram based on a TEM micrograph, illustrates the trapping of threading dislocations by SiO₂ sidewalls 325, with the dislocations terminating at the sidewalls in the lower portion of the ART regions.

[0042] Referring to Figure 9, a lower region of Ge containing the dislocations may be removed. The upper region, after removal of the substrate 300 and dislocation 610 regions, may be free of defects. The Ge in the upper regions may contain no threading dislocations due to lattice-mismatch, no stacking faults, no twins (two-dimensional lattice imperfections), and no cracks.

[0043] Figure 10 illustrates trenches filled with a crystalline material, e.g., GaAs, between dielectric, e.g., SiO₂, sidewalls on substrate 300, e.g., Si. The threading dislocations 610 slant towards the sidewall 325 near the bottom of the trenches. The GaAs is free of defects above the dashed line. The use of ART has been confirmed for the deposition of high-quality III-V materials on Si substrates, thereby confirming its viability for creating high-efficiency, low-cost multi-junction solar cells on Si substrates.

[0044] Analysis has shown that mismatch of thermal expansion coefficients generally does not cause cracking when growing lattice-mismatched materials using ART. The absence of cracking may be due to one or more of the following:

- The stresses are small because the epitaxial layers are thin.
- The material may elastically accommodate stresses arising from thermal-expansion mismatch because the trenches are relatively narrow, in contrast to very wide trenches, in which material behavior may approximate that of a bulk film.
- The dielectric material of the sidewall, e.g., SiO₂, tends to be more compliant than the semiconductor materials, and may serve as an expansion joint, stretching to accommodate the stress.

[0045] Referring again to Figure 2, the lattice and bandgap parameters of an embodiment of a solar cell with three junctions made from $\text{In}_{0.5}\text{Ga}_{0.5}\text{P}$ (1.86 eV), Si (1.15 eV), and $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ (0.61 eV) are illustrated. This solar cell has a theoretical maximum efficiency of 63.2%. This figure indicates that a device using InGaP material with 50% indium and 50% gallium is shown, but other concentrations of indium and gallium may be used to tune the bandgap and lattice constant of the material to improve the solar cell performance. The same is true for the InGaAs layer; the bandgaps for 70% indium and 30 % gallium are shown, but other fractions of indium and gallium may be used in the InGaAs layer to tune the bandgap and lattice constant for improved performance. For example, it may be desired to use an InGaAs layer lattice-matched to InP, as described below, and in this case, $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ may be used.

[0046] Figure 11 shows a three-junction solar-cell structure 1100 including a top ART region 1110 including InGaP regions with p-n junctions formed on the top of a silicon substrate 300 by ART, a p-n junction 1120 within the silicon substrate, and a bottom ART region 1130 including InGaAs regions with p-n junctions defined on the bottom surface of the silicon substrate by ART. The structure may incorporate tunnel junctions to make electrical contact between the three sub-cells, i.e., the top ART region, the substrate, and the bottom ART region.

[0047] In particular, the top ART region 1110 may function as a first defect-trapping layer including a first crystalline material 330 (e.g., InGaP) proximate and in contact with a first non-crystalline material 310 (e.g., SiO_2). The first crystalline material includes defects 610 arising from a lattice-mismatch of the first crystalline material to a first adjacent material (e.g., the Si substrate 300); the defects terminate at the first non-crystalline material 310. The top ART region 1110 may include a wetting layer 1140 of, e.g., p^+GaAs . The composition of the wetting layer 1140 is selected such that it forms a high-quality, continuous layer over the underlying material, e.g., Si, to allow the subsequent growth of the first crystalline material, e.g., InGaP. The top ART region may also include a base 1145 of, e.g., p InGaP, and an emitter 1150 of, e.g., n^+InGaP . InGaP may be selected because it has an appropriate bandgap. A photovoltaic junction 1152 is defined by the interface between the base 1145 and the emitter 1150. The InGaP material and In and Ga fractions are chosen so that the material has a bandgap of about 1.86 eV. This bandgap is chosen so that the top sub-cell absorbs high energy photons efficiently but allows lower energy photons to pass through undisturbed. The emitter is highly doped n-type to provide low resistance from the InGaP to the top contact metal. The

base is lightly doped p-type so that the InGaP has a high minority-carrier lifetime, which is preferred so that electron-hole pairs do not recombine before they are separated by the p/n junction. The top ART region may have a thickness of e.g., about 1 to 5 μm . A top contact layer 1155, e.g., a conductive material such as NiAu, may be disposed over the top ART region.

[0048] The bottom ART region 1130 may function as a second defect-trapping layer disposed below the first defect-trapping layer; the second defect-trapping layer includes a second crystalline material 330' (e.g., InGaAs) proximate and in contact with a second non-crystalline material 310' (e.g., SiO_2). The second crystalline material includes defects 610' arising from a lattice-mismatch to a second adjacent material (e.g., the Si substrate); the defects terminate at the second non-crystalline material 310'. The bottom ART region 1130 may include a wetting layer 1140' of, e.g., n^+GaAs , a bottom trapping region 1160 of, e.g., n^+InP , an emitter 1150' of, e.g., n^+InGaAs , and a base 1145' of p InGaAs, with a photovoltaic junction 1152' defined by an interface between the emitter 1150' of, e.g., n^+InGaAs and the base 1145' of, e.g., p InGaAs. The bottom ART region 1130 may have a thickness of e.g., about 1 to 5 μm . A bottom contact layer 1155', e.g., a conductive material such as NiAu, may be disposed over the bottom ART region.

[0049] A solar cell, i.e., p-n junction 1120, may be disposed between the top and bottom defect-trapping layers, e.g., in the Si substrate, defined with n^+ and p^+ doping. The p-n junction may be defined, e.g., by an emitter 1167 of n^+ Si formed by, for example, ion implantation, in a p-type Si substrate, with the remainder of the substrate defining a base 1168, the p-n junction 1120 being disposed between the emitter and the base.

[0050] A tunnel junction 1170 may be formed between the substrate 300 and the top ART region, and another tunnel junction 1170' may be formed between the substrate and the bottom ART region. A tunnel junction is a very highly doped p^+/n^+ diode. The doping is sufficiently high for current to tunnel between the p^+ and n^+ layers, with the tunnel junction forming a low resistance contact between two adjacent layers. In other words, the doping is sufficiently high such that the p^+/n^+ junction depletion region is small enough for tunneling to occur when the top ART region is exposed to light and, therefore, current flows through the top ART region. The current forward biases the tunnel junction. The tunnel junctions may be formed in III-V materials formed above and below the semiconductor substrate 300. By in-situ doping during

growth, high p^+ and n^+ doping of such layers may be achieved, e.g., above approximately $1 \times 10^{19} / \text{cm}^3$. A preferred tunnel junction may be selected such that a depletion region thickness is about 10 nm. As illustrated, in an embodiment, tunnel junctions 1170, 1170' may be defined in the top and bottom portions of a Si substrate 300. Then the doping in the silicon starting

5 from the top of the silicon substrate may be as follows:

p^{++} (tunnel junction) 1170

n^{++} (tunnel junction) 1170

n^+ (emitter) 1167

p (base) 1168

10 p^{++} (tunnel junction) 1170'

n^{++} (tunnel junction) 1170'

[0051] A structure may include additional solar cells disposed, e.g., below the second defect-trapping layer or above the first defect-trapping layer. In some embodiments, both the first and the second defect-trapping layers are disposed above a substrate.

15 **[0052]** In various embodiments, a large array (~500,000 on a 12-inch substrate) of trenches 300 nm to 500 nm wide covers the surface of each die on a Si substrate. In other embodiments, the trench width can vary over a broader range, such as from 180 nm to 5 μm . The distance between the trenches may be about 150 nm, below the wavelength of almost all of the solar radiation. This configuration may prevent solar radiation from passing between the trenches;

20 therefore, the cell may absorb almost all of the incident light. While the ~150 nm spacing is preferable for some criteria, the spacing may be substantially adjusted, based on application and/or material requirements.

[0053] The ART based 3-junction solar-cell structure shown in Figure 11 operates as follows.

- 25
- Sunlight first strikes the InGaP material 330 of the top ART cell 1110. InGaP absorbs photons with an energy of 1.82 eV or higher. Photons with an energy below 1.82 eV pass through the InGaP and enter the Si Substrate 300.
 - The photons that pass through the InGaP enter the top defect-trapping region 1165. Preferably, absorption in this region is avoided or reduced because photogenerated
- 30 carriers may recombine at the threading dislocations 610. Because most of the top

trapping region is created from InGaP, the trapping region will be transparent to the photons not absorbed by the region of InGaP above. While a wetting layer 1140 of GaAs is provided to facilitate two-dimensional growth of InGaP above the Si, this layer is kept very thin to reduce absorption of photons passing through to the Si. Those of skill in the art will understand how to apply other materials to decrease absorption by the wetting layer.

- Si absorbs photons with an energy of 1.15 eV or higher. Photons with an energy below 1.15 eV pass through the Si substrate 300.
- The photons that pass through the Si enter a second trapping region, i.e., bottom trapping region 1160. Again, the goal is to avoid absorption in this region because photogenerated carriers may recombine at the threading dislocations. Therefore, the trapping region is preferably created from InP, a high-bandgap material. The low-energy (≤ 1.15 eV) photons pass through the InP trapping into the InGaAs region. Since InP grows in a non-planar mode on Si, a thin GaAs wetting layer is preferably formed on the Si to grow two-dimensional layers of InP. The GaAs does not absorb the low-energy photons in this region because it has a wide bandgap.
- The InGaAs will then absorb photons with an energy of 0.61 eV or higher, and the p-n junction in the InGaAs will separate the photogenerated electron-hole pairs.

[0054] As described above, light will pass through a trapping region in an ART solar cell. Dislocations may cause absorption of sub-bandgap photons, but this sub-bandgap absorption does not significantly affect the performance of an ART-based cell.

[0055] In the trapping regions, threading dislocations create electron states within the bandgap. The material therefore absorbs some percentage of the sub-bandgap photons that pass through the trapping regions. Since the photogenerated carriers appear near threading dislocations, they tend to recombine non-radiatively and, i.e., without contributing to the solar cell's output power. It is possible to estimate the impact of this loss mechanism with the following equation that gives the transmission T as a function of the absorption coefficient α and the thickness t :

$$T = e^{-\alpha t}$$

[0056] It has been reported that the absorption coefficient of InP and GaAs regions grown on silicon is approximately 5×10^3 / cm for photons with energies between 0 and 0.5 eV below the bandgap. For devices in which the thickness of the highly dislocated regions is about 100 nm, which may be typical for ART trenches having a width on the order of 500 nm or less, the transmission through the trapping regions is expected to be about 95%.

[0057] It is possible to estimate the effect of this phenomenon on the efficiency of the three-junction solar cell described herein. The InGaP absorbs about 33% of the photons before any of them enter a trapping region. The remaining 67% of the photons enter the trapping regions in the InGaP cell. The trapping regions in the InGaP cell nominally absorb about 5% of that 67%, or about 3.3% of all the incident solar photons.

[0058] The remaining photons then pass through the silicon cell before they enter the trapping region in the InGaAs cell. By this time, the two upper (InGaP and Si) cells have absorbed about 67% of all the incident solar photons. Only 33% of the total incident solar photons reach the trapping region in the InGaAs cell. The trapping regions nominally absorb about 5% of that 33%, or about 1.7% of all the incident solar photons.

[0059] In total, then, the trapping regions absorb $\sim 3.3\% + \sim 1.7\% = \sim 5\%$ of all the incident photons. These simple calculations indicate that photon absorption in sub-bandgap regions near the threading dislocations may be a minor loss mechanism that may prevent ART solar cells from attaining their maximum theoretical efficiency of 63%, but does not preclude a production efficiency in excess of 50%.

[0060] The use of ART in solar cells may reduce the detrimental effect of dislocations. In bulk material, a dislocation can induce recombination over a relatively long distance, e.g., up to about 10 μm . The use of ART to make solar cells in trenches 300 to 500 nm wide reduces the sphere of influence of a defect significantly in comparison to a defect's influence in a bulk material or a film, since a dislocation cannot induce recombination in an adjacent trench.

[0061] The formation of InGaP and InGaAs on silicon using ART is an important part of the fabrication process used to create the triple junction cell shown in Figure 11. Techniques for forming InGaP and InGaAs on silicon using ART are now described in greater detail.

[0062] Figure 12 illustrates an embodiment of an ART structure for growing InGaP. A suitable Si substrate 300 may be obtained, for example, from ATDF, a subsidiary of SEMATECH. Illustratively, p-type Si (001) substrates are offcut by 6° to avoid anti-phase domain boundaries. A relatively thick dielectric layer 310, e.g., a thermal oxide having a thickness of 1 to 1.5 μm, is formed on the substrate. A trench 320 having a width of, e.g., 0.2 to 2.5 μm, is patterned in the thermal oxide by photolithography and dry etching.

[0063] After the patterning step, fluorocarbon residue may be removed from the substrate surface by an oxygen plasma ashing step (800 W at 1.2 Torr for 30 minutes in an oxygen plasma asher. The residue removal may be performed in, e.g., an ASPEN STRIP II system manufactured by Mattson Technology, Inc., based in Fremont, CA. The patterned substrate is cleaned, for example in Piranha, SC2, and dilute HF solutions sequentially. Epitaxial lattice-mismatched material 330 is selectively formed in the trench by, e.g., metal-organic chemical vapor deposition (MOCVD). The epitaxial lattice-mismatched material 330 may include InGaP disposed over a wetting layer 1140 of GaAs.

[0064] Figure 13 shows three possible growth modes of lattice-mismatched material 330. In the Frank-Van der Merwe (FM) mode, the material 330 grows over a substrate 300 in two dimensions, layer by layer. In the Volmer-Weber (VW) mode, interfacial energies cause isolated patches of epitaxial material 330 to grow and then coalesce. In the Stranski-Krastanov (SK) mode, the material 330 grows layer by layer until it reaches a critical thickness, and then it grows in patches.

[0065] InGaP tends to grow on Si in a non-planar mode, i.e., in either the second (VW) or third (SK) mode. Non-planar growth (i.e., VW or SK mode) typically leads to high concentrations of defects and a rough surface. In some embodiments, this issue is addressed by depositing a wetting layer 1140 of, e.g., GaAs directly onto the Si substrate before depositing the InGaP. The GaAs will grow in 2D layers on Si, and InGaP will grow in 2D layers on GaAs. Table 2 shows an exemplary set of conditions that may be adjusted for growing GaAs and InGaP.

Table 2: Initial Conditions for Deposition of GaAs Wetting Layer and InGaP

Material	Precursor Gases	Carrier Gas	Substrate Temp. (°C)	Reactor Pressure (Torr)	V-III Ratio	Growth Rate (nm/min)
GaAs	Triethyl Gallium (TEG), Arsine	H ₂	330-400	50-100	50-100	6
InGaP	Trimethyl Indium (TMI), TMG, Phosphine	H ₂	650-720	50-100	200-300	30

[0066] The V/III ratio is defined as the ratio between the flow rate of a group V element in the group V precursor to the flow rate of the group III element in the group III precursor, and may be calculated as (V precursor flow rate/III precursor flow rate) * (fraction of V element in V precursor/fraction of III element in III precursor). In summary, the V-III ratio is equal to the number of group V atoms/second that enter a processing chamber divided by the number of group III atoms/second that enter the processing chamber.

[0067] Growth conditions may be adjusted in a variety of ways, such as, for example:

- A pre-epitaxy bake of the substrate, e.g., in a temperature range of 800° to 1000°C.
- During growth, thermal cycle anneal at temperatures from room temperature to 800°C.
- To mitigate potential stacking fault defects as a result of thermal expansion coefficient mismatches between different materials such as InGaP, Si, and SiO₂, treat one or more of the materials to change its thermal expansion properties, e.g., subject the SiO₂ to a thermal nitrogen treatment to render its thermal expansion coefficient closer to that of Si.

[0068] In some embodiments, such as the three-junction solar-cell structure depicted in Figure 11, a high-bandgap InP trapping region may be interposed between the Si substrate and the InGaAs to avoid photon absorption in the trapping region of the lowest solar cell. The bandgap of the trapping region is preferably significantly higher than the bandgap of the sub-cell below the trapping region. If photons are absorbed in the trapping region, they do not convert into electrical energy because they recombine in the dislocations in the trapping region. If the trapping region bandgap is large, photons tend to pass through it and are absorbed efficiently by an underlying the sub-cell.

[0069] While in the foregoing discussion, InP, rather than another high-bandgap material is interposed, because InGaAs is nearly lattice-matched to InP, those of skill in the art will appreciate how to apply other suitable materials.

[0070] Figure 14 illustrates a structure in which a first crystalline material 330, e.g., wide bandgap InP, is formed over a GaAs wetting layer 1140 disposed in a trench 320. Subsequently, another crystalline material 1400, e.g., InGaAs, is formed over the first crystalline material, e.g., InP. InP is used to trap defects, and has a large bandgap, so light is not absorbed in it. The InGaAs functions as a solar cell. Table 3 sets forth an exemplary set of conditions that may be adjusted for growing InP and InGaAs.

Table 3: Initial Conditions for Deposition of InP and InGaAs

Material	Precursor Gases	Carrier Gas	Substrate Temp. (°C)	Reactor Pressure (Torr)	V-III Ratio	Growth Rate (nm/min)
InP	TMI, PH ₃	H ₂	620-720	70	100-200	30
InGaAs	TMI, TMG, AsH ₃	H ₂	550-580	70	100-250	30

[0071] Figure 15 shows an exemplary architecture for a single-junction InGaP solar cell 1500. Note that Figure 15 and other drawings of solar cells herein are schematics, rather than precise drawings. They omit, for example, contact doping regions, window layers, and back surface field layers, whose presence would be readily apparent to those of skill in the art.

[0072] The single-junction solar cell 1500 includes a top ART region 1110, as discussed with reference to Figure 11, and p⁺GaAs wetting layer 1140 disposed in a trench 320 over a p⁺Si substrate 300. A base layer 1145 of p InGaP is disposed over the wetting layer, and an emitter layer 1150 of n⁺InGaP is disposed over the base layer, defining a photovoltaic junction 1152 therebetween. The top ART region may have a thickness of e.g., about 1 to 5 μm. A top contact layer 1155, e.g., a conductive material such as NiAu, may be disposed over the top ART region. A bottom contact layer 1155', e.g., an Al layer, may be formed on the side of the Si substrate opposite the top ART region. The metals for the top and bottom contact layers are preferably selected to provide a low contact resistance with the adjacent semiconductor material. For example, aluminum provides a low contact resistance with doped silicon but not

with III-V materials. Thus, aluminum is preferably used as a contact layer adjacent to doped silicon. The Si substrate 300 may be doped p^+ and have a thickness of about 200 to 700 μm , with a preferred thickness of about 300 μm . Sunlight may impinge on the single-junction solar cell 1500 through the top contact layer 1155.

5 [0073] Trench widths, the layer thicknesses, and the doping levels may be varied to increase efficiency. In some embodiments, the InGaP thickness is between about 1 to 1.5 μm . Those of skill in the art will recognize how to adjust the geometrical structure of the device, the doping levels, and the material coefficients, without undue experimentation for a particular application.

[0074] Figure 16 shows an architecture for a single-junction InGaAs solar cell 1600. As
10 with the InGaP solar cell, trench widths, layer thicknesses and doping levels may be tailored to increase efficiency.

[0075] The single-junction InGaAs solar cell 1600 includes a bottom ART region 1130, as discussed with reference to Figure 11, formed on an n^+ Si substrate 300. The bottom ART region 1130 may include a wetting layer 1140' of, e.g., n^+ GaAs, a bottom trapping region 1160
15 of, e.g., n^+ InP, an emitter 1150' of, e.g., n^+ InGaAs, and a base 1145' of p InGaAs, with a photovoltaic junction 1152' defined by an interface between the emitter 1150' and base 1145'. The bottom ART region 1130 may have a thickness of e.g., about 1 to 5 μm . A bottom contact layer 1155', e.g., a conductive material such as NiAu, may be disposed over the bottom ART region. A top contact layer 1155, e.g., an Al layer, may be formed on the side of the Si
20 substrate opposite the bottom ART region. Sunlight may impinge on the single-junction solar cell 1600 through the top contact layer 1155.

[0076] In some embodiments the InGaAs thickness is between about 1 to 3 μm . The bottom ART region 1130 may have a thickness of 1 – 5 μm . The substrate may have a thickness of about 300 μm . Those of skill in the art will readily appreciate how to adjust the geometrical
25 structure of the device, the doping levels, and the material coefficients to optimize device performance for a particular application.

[0077] Figure 17 illustrates an embodiment of a dual-junction InGaP / Si cell 1700 and Figure 18 illustrates an embodiment of a dual-junction InGaAs / Si cell 1800. The dual-junction InGaP / Si solar cell 1700 includes a top ART region 1110 as described with reference
30 to Figure 11 and having a first photovoltaic junction 1152, disposed over a substrate 300

defining a second junction. In particular, the substrate may be p-type Si, having a thickness of about 300 μm . An emitter region 1705 of n^+Si may be formed in the substrate 300 by ion implantation. A base 1710 may be defined by the remainder of the substrate 300. Thus, a second photovoltaic junction 1720 is formed between the emitter 1705 and the base 1710. A tunnel junction 1170 may be disposed between the top ART region 1110 and the emitter 1705. A bottom metal layer 1155', e.g., Al, is formed on a backside of the substrate 300. The top ART region 1110 may be formed adjacent to the emitter 1705.

[0078] The dual junction solar cell 1800 of Figure 18 includes a first photovoltaic cell including a first semiconductor material having a first lattice constant and a first bandgap energy, e.g., Si. The first photovoltaic cell corresponds to the Si substrate 300, which includes an emitter 1705 of n^+Si , a base 1710 of p-type Si, and a photovoltaic junction 1720. A second photovoltaic cell includes a second semiconductor material having a second lattice constant different from the first lattice constant and a second bandgap energy lower than the first bandgap energy. The second photovoltaic cell may be formed adjacent to the base 1710 in, e.g., InGaAs, in a bottom ART region 1130, as described with reference to Figure 11. In particular, the second photovoltaic cell may include an emitter 1150' of n^+InGaAs and a base 1145' of p InGaAs, with a junction 1152' formed at the interface between the emitter and the base.

[0079] A defect-trapping layer 1160 is disposed between the first and second photovoltaic cells. The defect-trapping layer includes, e.g., n^+InP , a material having a third bandgap energy higher than the second bandgap energy. The defect-trapping layer includes a crystalline material (e.g., InP) proximate a non-crystalline material 310 (e.g., SiO_2), with the crystalline material including defects terminating at the non-crystalline material.

[0080] In an alternative to the structures illustrated in Figures 15 and 16, a solar cell architecture may include a film that is grown until it overflows the trench 320, as illustrated in Figure 19, to create an ART buffer layer 1900. The illustrated embodiment depicts a single-junction ART solar cell 1905 incorporating the ART buffer layer 1900. Adjacent discrete regions of lattice-mismatched material coalesce to form a single continuous film, i.e., the ART buffer layer 1900. A solar cell p-n junction is then grown on the buffer layer. The solar cell p-n junction may include a base 1910 and an emitter 1920, with a metal 1930 disposed thereover. The total thickness of the emitter, base, and dielectric layer may be about 1 to 5 μm . The

structure may be formed on a substrate 300, e.g., Si, having a thickness of approximately 300 μm . In embodiments based on ART buffer layers, as illustrated by the example of Figure 19, sidewall recombination does not diminish the solar cell performance because the active regions of the solar cell do not reside in the trench 320.

5 [0081] Figure 19 also illustrates a coalescence defect 1940, the vertical dotted line emerging from the top of a SiO_2 sidewall 325. These types of defects may appear in a selectively grown epitaxial film above a certain percentage of the SiO_2 pedestals, which may vary as a function of deposition conditions. Exemplary methods to reduce the density of these coalescence defects include:

- 10
- adjusting the MOCVD conditions, and
 - reducing the density of the coalescence regions that may give rise to defects. To reduce the density of those regions, the length of the overgrowth area (L_{og} in Figure 19) may be increased, which means increasing the width of the SiO_2 pedestals.

[0082] As L_{og} increases, a smaller percentage of the lower-energy light passing into the Si and InGaAs areas has to pass through the trapping regions. As a result, this architecture is less
15 vulnerable to sub-bandgap light absorption by dislocations within the trapping regions.

[0083] In some embodiments, the ART buffer layer is formed from the primary solar cell material; e.g., InGaP on the top and InGaAs on the bottom. Before growing other materials on the buffer layer, it may be desirable to planarize the buffer layer 1900. Tailoring of key
20 parameters for a planarization process employing chemical-mechanical-polishing (CMP) for InGaP and InGaAs may include selecting:

- a slurry that attacks the surface and weakens chemical bonds,
- the size and material of the abrasive particles,
- the hardness of the pad,

25

- the down force,
- the rotational speed,
- the duration of the treatment, and
- a suitable post-CMP cleaning step.

[0084] Figure 20 shows an alternative embodiment that uses a coalesced buffer region to form a three-junction InGaP/Si/InGaAs cell 2000. A single-junction ART solar cell 1905 incorporates a ART buffer layer 1900 that includes p⁺InGaP disposed over a wetting layer 1140 of p⁺GaAs formed in an opening defined in a dielectric material 310. A base 1910 of, e.g., p⁺InGaP is disposed over the buffer layer 1900, and an emitter 1920 of e.g., n⁺InGaP is disposed over the base, with a photovoltaic junction 2020 being formed at the interface between the emitter layer 1920 and the base 1910. The single-junction ART solar cell 1905 may have a thickness of e.g., 1 to 5 μm. A metal 1930 of, e.g., NiAu, is disposed over the single-junction ART solar cell 1930.

[0085] The single-junction ART solar cell 1930 is formed over a substrate 300 of, e.g., p-type Si, having a thickness of about 700 μm. An emitter region 2030 of, e.g., n⁺Si, is defined in the substrate, with the remainder of the p-type Si substrate defining a base 2040. Thus, a second photovoltaic junction 2020' is defined by an interface between the emitter 2030 and the base 2040. Tunnel junctions 1170, 1170' are formed on the top and bottom surfaces of the semiconductor substrate 300.

[0086] Finally, a second single-junction ART solar cell 1905' is disposed over a backside of the substrate 300, adjacent the base 2040. The cell 1905' includes a third photovoltaic junction 2020', disposed between an emitter 1920' of n⁺InGaAs and a base 1910' of p-type InGaAs. An ART buffer layer 1900' may be formed over a trapping layer 1160' of n⁺InP that is disposed over a wetting layer 1140' of n⁺GaAs.

[0087] Referring to Figures 21a–21j, an exemplary process for fabricating a three-junction InGaP / Si / InGaAs solar cell includes the following steps:

1. A crystalline semiconductor substrate 300 having a top surface 2100 and a bottom surface 2100', e.g., an 8- or 12-inch Si substrate, is provided. The substrate may be p-type, with an n⁺ region emitter 1705 implanted through the top surface, thereby defining an n⁺/p solar cell junction 2110 between the emitter 1705 and the base 1710 (defined by the remainder of the substrate 300). Alternatively, the n⁺ region emitter may be formed by epitaxial growth. The doping level for the n⁺ emitter may be relatively high, e.g., greater than $1 \times 10^{19} / \text{cm}^3$, while the doping level for the base may be relatively low, e.g., less than $1 \times 10^{16} / \text{cm}^3$. A top protective layer 2115, e.g., a layer of SiN_x having a thickness of e.g., 200 nm, is formed on the top substrate surface 2100.

2. The bottom surface 2100' or backside of the substrate is implanted with a p-type dopant, e.g., boron at a dose of 1×10^{14} to $2 \times 10^{15}/\text{cm}^2$, preferably $1 \times 10^{15}/\text{cm}^2$, with an energy of 5 to 20 keV energy, preferably 10 keV, 7° tilt, to form a thin p^+ region, and then an n-type dopant, e.g., arsenic at a dose of $2 \times 10^{15}/\text{cm}^2$ to $5 \times 10^{15}/\text{cm}^2$, preferably $5 \times 10^{15}/\text{cm}^2$,
5 with an energy of 10 to 60 keV, preferably 20 keV, 7° tilt, thereby defining a tunnel junction 1170. The dose, and energy of the two implants should be optimized so that the voltage drop across the tunnel junction is minimized for a given current. The n^+ region is preferably shallow so that it does not compensate the deeper p^+ region.
3. A bottom insulator layer 310' is formed proximate the bottom surface 2100' of the
10 substrate by, e.g., depositing a 1 to 5 μm layer of SiO_2 on the backside of the substrate by CVD. A plurality of bottom openings 320', i.e., ART trenches, are formed through the bottom insulator layer by creating ART trenches in the SiO_2 are formed by lithography and dry etch.
4. A second crystalline layer, i.e., a second lattice-mismatched material 330' is formed
15 within the bottom openings by, e.g., growing an n^+ GaAs/InP buffer layer with a thickness between 10 nm and 1 micron (~ 400 nm) (including wetting layer 1140' and trapping layer 1160) and a p- and n-type InGaAs cell layer (1 to 5 μm) (including an emitter 1150' and base 1145', with photovoltaic junction 1152' disposed therebetween) in one step in the same MOCVD reactor. The second crystalline layer is lattice-mismatched to the
20 crystalline semiconductor substrate. A majority of defects arising at a surface of the second crystalline layer nearest the crystalline semiconductor substrate terminate within the respective bottom openings.
5. A bottom protective layer 2115', e.g., a layer of SiN_x having a thickness of about 200 nm, is deposited on the back side of the structure by CVD.
- 25 6. The top protective layer 2115 is removed from the top surface 2100 of the substrate by, e.g., dry etching. The substrate is cleaned with a suitable wet clean, e.g., piranha (sulfuric acid, H_2O_2 , and water) and an HF etch.
7. A top insulator layer 310 is formed proximate the top surface of the substrate by, e.g., depositing a 1 to 5 μm layer of SiO_2 on the top surface of the substrate by CVD. A
30 plurality of top openings 320 are defined in the top insulator layer by, e.g., the creation of ART trenches in the SiO_2 by lithography and dry etch.

8. A first lattice-mismatched material 330, i.e., a first crystalline layer, is formed within the top openings 320 by, e.g., growing a GaAs wetting layer 1140 and a InGaP base layer 1145 in one step in the same reactor. The first crystalline layer is lattice-mismatched to the crystalline semiconductor substrate. A majority of defects arising at a surface of the first crystalline layer nearest the crystalline semiconductor substrate terminate within the respective top openings.
9. A top protective layer 2115, e.g., a layer of SiN_x with a thickness of between 50 nm and 500 nm, preferably about 200 nm is deposited on the top side of the structure by CVD. The bottom protective layer 2115' is removed from the backside of the substrate by a dry etch and a wet clean with, e.g., piranha and HF dip.
10. A bottom metal 1155' is formed on the back side of the structure by e-beam deposition or sputtering. The bottom metal may include a suitable composition for forming a low resistance contact. For example, the bottom metal may include or consist of an Au/Ni alloy, having a thickness selected from a range of about 300 nm to about 1 μm , preferably about 500 nm.
11. The top protective layer 2115 is removed by, e.g., dry etching, and the top surface is cleaned with water. A top metal 1155 is deposited over the structure. The top metal may be a metal suitable for forming a low-resistance contact with the adjacent semiconductor material. A suitable metal is, for example, an Au/Ni alloy, with a thickness selected from a range of about 500 nm to about 1 μm . Contacts are patterned in the metal 1155 by photolithography and etch. Subsequently, an anneal with forming gas may be performed to improve the contacts. Forming gas is a mixture of up to 10% hydrogen in nitrogen; the anneal may be of sufficiently high temperature and duration to improve the contact, e.g., about 250 °C to 450 °C, preferably about 400 °C for about 1 second to 5 minutes, preferably 1 minute in a rapid thermal annealing system. The anneal may also be performed in a conventional furnace for a longer duration.

[0088] The resulting structure has a top ART region 1110, i.e., a first solar cell or photovoltaic cell, disposed above the substrate 300. The first solar cell includes a first semiconductor material having a first lattice constant, i.e., the first crystalline layer. The first semiconductor material includes a first III-V compound, and the first solar cell has a first photovoltaic junction 1152 defined by the III-V compound. A second solar cell or photovoltaic

cell is disposed below the first solar cell, e.g., defined in the substrate 300. The material of the second solar cell, e.g., silicon, has a second lattice constant mismatched with respect to the first semiconductor material. The second solar cell includes an emitter 1705 and a base 1710, with a second photovoltaic junction 2110 defined therebetween. A bottom ART region 1130, i.e., a
5 third solar cell or photovoltaic cell, is disposed below the second solar cell and below the substrate. The third solar cell includes the second semiconductor material that is lattice-mismatched to the material of the second solar cell, e.g., a second III-V compound, and a photovoltaic junction 1152'.

[0089] The first solar cell has a first energy bandgap, e.g., less than 1.1 eV; in some
10 embodiments, the first energy bandgap is less than about 0.8 eV. The second solar cell is disposed below the first solar cell and has a second energy bandgap greater than the first energy bandgap and approximately equal to a bandgap of silicon, i.e., 1.1 eV. The third solar cell is disposed below the second solar cell and has a third energy greater than the second energy bandgap, e.g., greater than 1.1 eV. In some embodiments, the third energy bandgap is greater
15 than about 1.6 eV.

[0090] Figure 22 illustrates a five-junction InGaP / GaAs / Si / GaAsSb / InGaAs solar cell
2200. Similarly to the embodiment illustrated in Figure 11, this embodiment uses ART on both sides of a Si substrate 300 that has a photovoltaic junction 2110 defined therein. ART is used to trap defects to facilitate forming two solar cells, i.e., a top ART cell 1110 containing GaAs
20 and a bottom ART cell 1130 containing GaAsSb, above the top and bottom surfaces of the Si substrate, respectively. A fourth photovoltaic cell 2210, e.g., an InGaP cell, is formed over the top ART GaAs cell, and a fifth photovoltaic cell 2220, e.g., an InGaAs cell, is formed over the GaAsSb cell. The crystal lattices for these latter cell pairs are substantially matched to adjacent materials and thereby avoid lattice-mismatch defects.

[0091] Figure 23 illustrates an embodiment in which ART is first used to form a first top
25 ART region 1110 that traps defects arising from lattice-mismatch for an InGaAs solar cell, which has a nominal bandgap of about 0.7 eV, grown above a silicon substrate 300. Then a second top ART region 1110' is formed over the first top ART region. The second top ART region includes a GaAs solar cell with a nominal bandgap of about 1.4 eV. Finally, a third
30 solar cell 2300, including, e.g., n- and p-type InGaP, which has a nominal bandgap of about 1.8 eV, is grown above the second top ART region 1110', i.e., over the GaAs cell.

[0092] As discussed above, fabrication of solar cell embodiments that have junctions on both sides of a substrate without using ART techniques is possible. While ART provides an excellent way to reduce defects arising from lattice-mismatch between different materials, those of skill in the art will, in view of the disclosure herein, understand how to use other techniques that have either suitable or tolerable defect levels. For example, Figure 24 shows the use of compositionally graded top and bottom buffer layers 2400, 2400', e.g., InGaP graded buffer layers formed on both sides of a substrate 300, e.g., a Si substrate, to facilitate a three-junction InGaP / Si / InGaAs solar cell. Illustratively the graded buffer layers 2400, 2400' each start with GaP formed adjacent the Si substrate (because GaP has a lattice constant that approximately matches that of Si). On a top side of the Si substrate, the graded buffer layer 2400 includes GaP and is graded to a layer of (approximately) $\text{In}_{0.5}\text{Ga}_{0.5}\text{P}$, and on a bottom side, the graded buffer layer 2400' includes GaP graded to an $\text{In}_x\text{Ga}_{1-x}\text{P}$ layer that has a lattice constant matched, at least approximately, to the lattice constant of InGaAs. In the illustrated structure, the graded buffer layers 2400, 2400' are disposed between the first (InGaP top photovoltaic cell 2410) and second (Si substrate 300 photovoltaic cell) photovoltaic cells, and the second (Si substrate 300) and third (InGaAs bottom photovoltaic cell 2410') photovoltaic cells, respectively. Those of skill in the art understand the criteria for the selection of materials and other parameters such as thicknesses and growth conditions for the graded buffer layers.

[0093] Those of skill in the art also understand how to apply techniques other than ART and graded buffers, such as wafer bonding, selective epitaxy on mesas, or direct epitaxy of lattice-mismatched materials, to facilitate creating solar cell junctions on both sides of a substrate. For example, Figures 25a and 25b illustrate an embodiment that uses wafer bonding or layer transfer to create a three-junction InGaP / Si / Ge solar cell 2500. A single-junction Si solar cell 2510 (i.e., a first active photonic device layer) and a single-junction Ge solar cell 2520 (i.e., a second active photonic device layer) are fabricated directly on Si and Ge substrates, respectively, by the implantation of appropriate dopants. An InGaP solar cell 2530 is formed on a GaAs substrate 2540. Wafer bonding techniques are then used to combine the Si, Ge, and InGaP solar cells 2510, 2520, and 2530 into a multi-junction solar cell 2500, with the GaAs substrate 2540 being removed, for example, by wet etching. For example, the first active photonic device layer may be formed in InGaP 2530 and bonded to a top surface of the Si substrate 2510 (including a solar cell). A second active photonic device layer may be formed in

Ge 2520 and bonded to a bottom surface of the Si substrate 2510. A third active photonic device layer may be defined by the Si substrate 2510. Figure 25b illustrates an embodiment with a current path that flows from the InGaP cell 2530 through the Si cell 2510 and into the Ge cell 2520.

- 5 [0094] In an alternative embodiment that does not require current matching between the three cells, a dielectric layer may be included between each of the cells, in which case separate electrodes are used for each of the three cells.

- [0095] In some embodiments, at least a portion of an ART region may be formed in, rather than over, a substrate. An exemplary process is illustrated in Figures 26a – 26f. A substrate
10 300, e.g., a Si wafer, is provided. A masking layer 2600 is formed over the substrate 300. The masking layer 2600 may include a thin layer of silicon dioxide 2610 and a thicker layer of silicon nitride 2620 disposed thereover. The silicon dioxide layer may be about 100 nm thick and the silicon nitride layer may be about 1000 nm. The silicon dioxide layer is interposed between the silicon nitride layer and the substrate to reduce cracking of the nitride layer. The masking
15 layer is patterned by a photolithographic patterning step, and openings 2630 are dry etched through the masking layer 2600 and into the substrate 300. The openings 2630 may be, e.g., trenches. The trench width may range from 20 nm to 20 μ m and the depth is selected such that the trench aspect ratio (the ratio of the depth to the width) is ≥ 1 . A second silicon dioxide layer 2640 is conformally deposited over the masking layer 2600 and along the sidewalls of the
20 openings 2630 or grown along the sidewalls of the openings 2630. A dry etch of the second silicon dioxide layer 2640 is performed, removing the second dioxide layer 2640 from the silicon nitride 2620 and from the bottom portions 2650 of the openings, and leaving the second silicon dioxide layer 2640 on the sidewalls 2660 of the openings. A thin layer, about between 10 and 100 nm, optimally 25 nm, of silicon dioxide may be grown over the silicon dioxide
25 portions 2620 and the exposed bottom portions of the openings, and subsequently removed by a dip in HF. This thin silicon dioxide layer is grown and stripped to clean the surface of the bottom of the trench, thereby removing damage and carbon compounds left over after the trench dry etch. The resulting structure includes openings 2630 defined in the substrate 300, with silicon dioxide layers 2610, 2640 disposed over the sidewalls of the openings and over the
30 top surface of the substrate 300. This configuration provides an exposed crystalline surface suitable for epitaxial growth (i.e., the exposed substrate material in the bottom portions of the

openings) and openings lined with a dielectric material, suitable for trapping defects by ART in lattice-mismatched crystalline material formed in the openings. Subsequently, lattice-mismatched material 330 may be formed in the openings, and used to form the solar-cell structures described above.

- 5 [0096] The invention may be embodied in other specific forms without departing from the spirit or essential characteristics thereof. The foregoing embodiments are therefore to be considered in all respects illustrative rather than limiting on the invention described herein.

[0097] What is claimed is:

What is claimed is:

- 1 1. A structure comprising:
 - 2 a semiconductor substrate having a top surface and a bottom surface;
 - 3 a top insulator layer disposed proximate the top surface of the substrate and defining a
 - 4 top opening;
 - 5 a bottom insulator layer disposed proximate the bottom surface of the substrate and
 - 6 defining a bottom opening;
 - 7 a first crystalline layer disposed within the top opening, the first crystalline layer being
 - 8 lattice-mismatched to the semiconductor substrate, a majority of lattice-mismatch defects
 - 9 arising at a surface of the first crystalline layer nearest the substrate terminating within the top
 - 10 opening; and
 - 11 a second crystalline layer disposed within the bottom opening, the second crystalline
 - 12 layer being lattice-mismatched to the semiconductor substrate, a majority of lattice-mismatch
 - 13 defects arising at a surface of the second crystalline layer nearest the substrate terminating
 - 14 within the bottom opening.
- 1 2. A structure comprising:
 - 2 a substrate;
 - 3 a first photovoltaic sub-cell formed above the substrate and including a first
 - 4 semiconductor material having a first lattice constant;
 - 5 a second photovoltaic sub-cell formed below the first photovoltaic sub-cell, the second
 - 6 photovoltaic sub-cell including a second semiconductor material having a second lattice
 - 7 constant different from the first lattice constant; and
 - 8 a third photovoltaic sub-cell formed below the second photovoltaic cell and below the
 - 9 substrate, the third photovoltaic sub-cell including a third semiconductor material having a
 - 10 third lattice constant different from the second lattice constant.
- 1 3. The structure of claim 2 wherein the first semiconductor material comprises a III-V
- 2 compound, and the first photovoltaic sub-cell comprises a first photovoltaic junction defined by
- 3 the III-V compound.
- 1 4. The structure of claim 2 wherein the second photovoltaic sub-cell comprises a second
- 2 photovoltaic junction defined in the substrate.

1 5. The structure of claim 2 wherein the first photovoltaic sub-cell comprises a first III-V
2 compound, the second photovoltaic sub-cell comprises silicon, and the third photovoltaic sub-
3 cell comprises a second III-V compound.

1 6. The structure of claim 2 wherein the substrate comprises silicon.

1 7. The structure of claim 2, further comprising a compositionally graded buffer layer disposed
2 between the first and second photovoltaic sub-cells.

1 8. The structure of claim 2, further comprising a defect-trapping layer disposed between the
2 first and second photovoltaic cells, the defect-trapping layer including (i) a crystalline material
3 comprising defects arising from lattice-mismatch of the crystalline material with an adjacent
4 semiconductor material and (ii) a non-crystalline material, the defects terminating at the non-
5 crystalline material.

1 9. A structure comprising:

2 a first photovoltaic sub-cell including a first semiconductor material having a first
3 lattice constant and a first bandgap energy;

4 a second photovoltaic sub-cell including a second semiconductor material having a
5 second lattice constant different from the first lattice constant and a second bandgap energy
6 lower than the first bandgap energy; and

7 a defect-trapping layer disposed between the first and second photovoltaic sub-cells, the
8 defect-trapping layer having a third bandgap energy higher than the second bandgap energy, the
9 defect-trapping layer including a crystalline material and a non-crystalline material, the
10 crystalline material comprising defects terminating at the non-crystalline material.

1 10. A structure comprising:

2 a first defect-trapping layer including a first crystalline material proximate and in
3 contact with a first non-crystalline material, the first crystalline material comprising defects
4 arising from a lattice-mismatch of the first crystalline material to a first adjacent material, the
5 defects terminating at the first non-crystalline material; and

6 a second defect-trapping layer disposed below the first defect-trapping layer, the second
7 defect-trapping layer including a second crystalline material proximate and in contact with a
8 second non-crystalline material, the second crystalline material comprising defects arising from

9 a lattice-mismatch to a second adjacent material, the defects terminating at the second non-
10 crystalline material.

1 11. The structure of claim 10 wherein the first and second defect-trapping layers are disposed
2 on opposite sides of a substrate, the substrate comprises the first and second adjacent materials,
3 and the first and second adjacent materials are the same.

1 12. The structure of claim 10 wherein the first and second defect-trapping layers are each
2 disposed above a substrate, the substrate comprises the first adjacent material, and the first
3 crystalline material comprises the second adjacent material.

1 13. The structure of claim 10, further comprising a solar sub-cell disposed between the first
2 and second defect-trapping layers.

1 14. The structure of claim 10, further comprising a solar sub-cell disposed below the second
2 defect-trapping layer.

1 15. The structure of claim 10, further comprising a solar sub-cell disposed above the first
2 defect-trapping layer.

1 16. The structure of claim 10, further comprising:

2 a first semiconductor layer having a first lattice constant disposed above the first defect-
3 trapping layer; and

4 a second semiconductor layer having a second lattice constant different from the first
5 lattice constant disposed above the second defect-trapping layer.

1 17. A method of forming a photonic device, the method comprising:

2 providing a substrate;

3 forming a first active photonic device layer above the substrate; and

4 forming a second active photonic device layer below the substrate,

5 wherein forming each of the first and second active photonic device layers comprises
6 epitaxial growth.

1 18. The method of claim 17 wherein the substrate includes a third photonic device layer.

1 19. The method of claim 17 wherein the first active photonic device layer comprises a first
2 solar cell junction and the second active photonic device layer comprises a second solar cell
3 junction.

- 1 20. A multi-junction solar cell device comprising:
2 a first solar sub-cell comprising a first non-Si photovoltaic junction;
3 a second solar sub-cell disposed below the first solar sub-cell and comprising a Si
4 photovoltaic junction; and
5 a third solar sub-cell disposed below the second solar sub-cell and comprising a second
6 non-Si photovoltaic junction.
- 1 21. A multi-junction solar cell device comprising:
2 a first solar sub-cell having a first energy bandgap;
3 a second solar sub-cell formed below the first solar cell and having a second energy
4 bandgap greater than the first energy bandgap and approximately equal to 1.1 eV; and
5 a third solar sub-cell formed below the second solar cell and having a third energy
6 bandgap greater than the second energy bandgap.
- 1 22. The multi-junction solar cell device of claim 21, wherein the first energy bandgap is less
2 than 1.1 eV and the third energy bandgap is greater than 1.1 eV.
- 1 23. The multi-junction solar cell device of claim 22 wherein the first energy bandgap is less
2 than about 0.8 eV.
- 1 24. The multi-junction solar cell device of claim 21 wherein the second bandgap is selected
2 from a range of about 1.0 eV to about 1.2 eV.
- 1 25. The multi-junction solar cell device of claim 21 wherein the third energy bandgap is
2 greater than about 1.6 eV.