

200005182-1



PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁶ : H04L 25/06, 25/02		A1	(11) International Publication Number: WO 99/48260	
			(43) International Publication Date: 23 September 1999 (23.09.99)	
(21) International Application Number: PCT/US99/05120		(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, GH, GM, HR, HU, ID, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).		
(22) International Filing Date: 8 March 1999 (08.03.99)		Published <i>With international search report.</i>		
(30) Priority Data:				
60/078,213	16 March 1998 (16.03.98)			US
09/057,158	7 April 1998 (07.04.98)			US
09/165,705	2 October 1998 (02.10.98)	US		
(71) Applicant (for all designated States except US): JAZIO, INC. [US/US]; 864 Talisman Drive, Sunnyvale, CA 94087 (US).				
(72) Inventor; and				
(75) Inventor/Applicant (for US only): EJAZ, UI, Haq [-/US]; 864 Talisman Drive, Sunnyvale, CA 94087 (US).				
(74) Agents: SOCKOL, Marc, A. et al.; Graham & James LLP, 600 Hansen Way, Palo Alto, CA 94304-1043 (US).				

(54) Title: HIGH SPEED SIGNALING FOR INTERFACING VLSI CMOS CIRCUITS

(57) Abstract

A system of the present invention uses small swing differential source synchronous voltage and timing reference (SSVTR and /SSVTR) signals to compare single-ended signals of the same slew rate generated at the same time from the same integrated circuit for high frequency signaling. The SSVTR and /SSVTR signals toggle every time the valid signals are driven by the transmitting integrated circuit. Each signal receiver includes two comparators, one for comparing the signal against SSVTR and the other for comparing the signal against /SSVTR. A present signal binary value determines which comparator is coupled to the receiver output, optionally by using XOR logic with SSVTR and /SSVTR. The coupled comparator in the receiver detects whether change in signal binary value occurred or not until SSVTR and /SSVTR have changed their binary value. The same comparator is coupled if the signal transitions. The comparator is de-coupled if no transition occurs. The system may use a first set of oscillating references on a first bus for detecting transitions in control information and a second set of oscillating references for detecting transitions in data information.

