CLAIMS

1. An electronic device, comprising:

an antenna; and

a transceiver communicatively coupled to the antenna, the transceiver comprising a plurality of amplification circuits, each amplification circuit of the plurality of amplification circuits comprising

a first transistor,

a second transistor,

a third transistor having a gate coupled to a gate of the first transistor, and a drain coupled to a drain of the second transistor,

a fourth transistor having a gate coupled to a gate of the second transistor, a drain coupled to a drain of the first transistor, and a source coupled to a source of the first transistor, the source of the third transistor and the source of the fourth transistor being coupled to a resistive component, and

a switch configured to couple an amplification circuit of the plurality of amplification circuits to an operating circuit of the electronic device to vary a gain of the plurality of amplification circuits.

2. The electronic device of claim 1, wherein the third transistor of a respective amplifier is configured to neutralize a first parasitic capacitance of the first transistor of the respective amplifier with a second parasitic capacitance of the third transistor when the first transistor exhibits the first parasitic capacitance.

3. The electronic device of claim 1, wherein the fourth transistor of a respective amplifier is configured to neutralize a first parasitic capacitance of the second transistor of the respective amplifier with a second parasitic capacitance of the fourth transistor when the second transistor exhibits the first parasitic capacitance.

4. The electronic device of claim 1, wherein the resistive component is coupled to ground.

5. The electronic device of claim 4, wherein the resistive component is configured to block current flow from the source of the third transistor and the source of the fourth transistor to the ground.

6. The electronic device of claim 1, wherein the resistive component is coupled to the source of the first transistor and a source of the second transistor.

7. The electronic device of claim 1, wherein the resistive component, the source of the first transistor, and a source of the second transistor are coupled to the switch.

8. A transceiver, comprising:

a plurality of amplifiers, each amplifier of the plurality of amplifiers comprising a plurality of amplification circuits, each amplification circuit of the plurality of amplification circuits comprise

a first amplifying transistor,

a second amplifying transistor,

a first neutralizing transistor having a gate coupled to a gate of the first amplifying transistor, and a drain coupled to a drain of the second amplifying transistor,

a second neutralizing transistor having a gate coupled to a gate of the second amplifying transistor, a drain coupled to a drain the first amplifying transistor, and a source coupled to a source of the first neutralizing transistor, the source of the first neutralizing transistor and the source of the second neutralizing transistor being coupled to a resistor, and,

a switch configured to couple an amplification circuit of the plurality of amplification circuits to an operating circuit of the electronic device to vary a gain of the plurality of amplification circuits, and

a plurality of matching networks communicatively coupled to the plurality of amplifiers.

9. The transceiver of claim 8, wherein, in operation, the first neutralizing transistor exhibits a first parasitic capacitance between the gate of the first neutralizing transistor and the drain of the first neutralizing transistor, a second parasitic capacitance between the gate of the first neutralizing transistor and the source of the first neutralizing transistor, and a third parasitic capacitance between the drain of the first neutralizing transistor and the source of the first neutralizing transistor.

10. The transceiver of claim 9, wherein a first matching network of the plurality of matching networks communicatively coupled to an amplifier of the plurality of amplifiers is configured to absorb the second parasitic capacitance, and a second matching network of the plurality of

matching networks communicatively coupled to the amplifier is configured to absorb the third parasitic capacitance.

11. The transceiver of claim 10, wherein each amplifier is configured to neutralize a parasitic capacitance of the first amplifying transistor with the first parasitic capacitance.

12. The transceiver of claim 8, wherein the resistor comprises a variable resistor.

13. Amplification circuitry, comprising:

a first transistor;

a second transistor;

a third transistor having a gate coupled to a gate of the first transistor, and a drain coupled to a drain of the second transistor;

a fourth transistor having a gate coupled to a gate of the second transistor, a drain coupled to a drain of the first transistor, and a source coupled to a source of the third transistor, the source of the third transistor and the source of the fourth transistor being coupled to a resistor; and

a switch configured to couple the amplification circuity of a plurality of amplification circuits to an operating circuit of an electronic device to vary a gain of the plurality of amplification circuits.

14. The amplification circuitry of claim 13, wherein the amplification circuitry is configured to cancel a voltage swing received at the source of the first transistor or the third transistor with a voltage swing received at the source of the second transistor or the fourth transistor.

15. The amplification circuitry of claim 13, wherein the amplification circuitry is configured to neutralize a parasitic capacitance of the first transistor with a parasitic capacitance of the third transistor.

16. The amplification circuitry of claim 15, wherein the parasitic capacitance of the first transistor is exhibited between the gate of the first transistor and the drain of the first transistor, and the parasitic capacitance of the third transistor is exhibited between the gate of the third transistor and the drain of the third transistor.

17. The amplification circuitry of claim 13, wherein the amplification circuitry is configured to neutralize a parasitic capacitance of the second transistor with a parasitic capacitance of the fourth transistor.

18. The amplification circuitry of claim 17, wherein the parasitic capacitance of the second transistor is exhibited between the gate of the second transistor and the drain of the second transistor, and the parasitic capacitance of the third transistor is exhibited between the gate of the third transistor and the drain of the third transistor.

19. The amplification circuitry of claim 13, wherein the amplification circuitry is configured to amplify a signal having a frequency of 24 gigahertz or greater.

20. The amplification circuitry of claim 19, wherein a gain of the signal amplified by the amplification circuitry is 17 decibels or greater.