

Description

The invention relates to a phase detector that may be used in a phase-lock-loop circuit of, for example, a digital television apparatus.

In a digital television receiver, for example, it may be desirable to generate the deflection current using a phase-lock-loop circuit (PLL). A periodic output signal of the PLL that is used for driving, for example, a horizontal output stage is synchronized to an incoming synchronizing signal such as the horizontal sync pulses of a baseband television signal.

Unlike in an analog PLL circuit that utilizes a voltage controlled oscillator (VCO) having a controllable frequency, it may be desirable to operate the PLL circuit of the digital television synchronously with a common system clock having, for example, a constant frequency.

The periodic output signal, generated by the digital PLL circuit, may include two parts: a first signal part that changes states or has a transition edge coincidental with the system clock and a second signal part that is indicative of a fraction of the clock period and that may be updated once in each cycle of the periodic signal. A timing edge of the periodic output signal may be defined to occur at an instant corresponding to the fraction of the clock period that follows the transition edge of the first signal part. The fraction of the clock period is determined in accordance with the second signal part. The information contained in the second signal part may be referred to as skew information. An example of a PLL that generates signals such as the first and second signal parts is described in U.S. Patent No. 4,639,780 in the name of D.H. Willis, entitled TELEVISION SYNCHRONIZING APPARATUS (the Willis patent).

In such digital phase-lock-loop circuit, the incoming synchronizing signals, such as, for example, the horizontal sync pulses of a baseband television signal, is sampled at the system clock rate and then digitized in an analog-to-digital converter. The resulting digitized synchronizing signal and the periodic output signal of the PLL are coupled to corresponding input ports of a phase detector of the digital PLL that generates a feedback, phase difference signal from the two signals.

For obtaining the phase difference signal, some prior art digital phase detectors utilize information obtained in each sampling period of the system clock throughout the duration of the sync pulse. Disadvantageously, a noise signal accompanying the sync pulse may affect, in such prior art detector, the phase difference signal any time throughout the sync pulse when such noise appears at the sampling instants.

It is herein recognized as desirable to reduce the effect of such noise signal by utilizing only samples that occur in the proximity of a transition edge within the sync pulse. In this way, a noise signal that occurs

at other sampling instants of the sync pulse, advantageously, will not substantially affect the phase difference signal.

Furthermore, it may be desirable to generate a correct phase difference signal even when the width of the given sync pulse or the period of the given sync pulse is not equal to an integer multiple of the sampling clock period.

In accordance with one aspect of the invention, there is provided a digital phase detector responsive to first and second input signals for generating a phase difference signal that is indicative of a phase difference therebetween, comprising: a source of a periodic clock signal; sampling means responsive to said first input signal and to said clock signal for sampling said first input signal to generate a sampled signal that contains first and second sampled values of said first input signal, each of said first and second sampled values being representative of said first input signal at corresponding first and second instants that occur synchronously with respect to said clock signal; characterized by computing means being responsive to said sampled signal for computing, by interpolation of said first and second sampled values, a third value that is representative of said first input signal at a third instant when a transition edge in said first input signal is estimated to occur, said computing means further being responsive to said second input signal for computing a difference between said third instant and a corresponding instant when a corresponding transition edge in said second input signal occurs to generate said phase difference signal in accordance with said difference.

In accordance with another aspect of the invention, there is provided a digital phase detector responsive to a first input signal having a pulse that includes first and second transition edges that change in opposite manner such that both said first and second transition edges define said pulse, and responsive to a second input signal for generating a phase difference signal that is indicative of a phase difference between said first and second input signals, comprising: a source of a periodic clock signal; sampling means responsive to said first input signal and to said clock signal for generating a sampled signal that contains a plurality of sample portions that are representative of corresponding levels in said first input signal; characterized by second means responsive to said sampled signal for selecting, from said plurality of sample portions, a first sample portion that is indicative of a first instant when said first transition edge occurs such that, in selecting said first sample portion, said second means excludes each sample portion of said plurality of sample portions that corresponds to any portion of said pulse that is not associated with said first transition edge, said second means being responsive to said second input signal for generating said phase difference in accordance with said second

input signal and in accordance with said first sample portion to the exclusion of the remaining ones of said plurality of sample portions.

In the Drawing:

FIGURE 1 illustrates a phase detector embodying the invention; and

FIGURES 2a-2g illustrate waveforms useful in explaining the operation of the phase detector of FIGURE 1.

FIGURE 1 illustrates a block diagram of a horizontal deflection circuit including a phase-lock-loop circuit (PLL) 20. It includes a sequential counter 21 that has the analogous function of a VCO of a conventional phase-lock-loop circuit. Counter 21 is a programmable counter that is incremented after each leading edge of a clock CK having a period t_{CK} , illustrated in the timing diagram of FIGURE 2a. It counts up, from an initial value of, for example, 1 until it is reset to the initial value by a reset pulse RESET at an input terminal 21a of FIGURE 1. Pulse RESET controls the number of clock CK periods t_{CK} that are included in a corresponding period, or sequence, N, of counter 21.

A signal CT, at an output port 21b of counter 21, supplies, in a given sequence N, the current count of counter 21 that occurs coincidentally with clock CK. A skew signal SK, generated by a skew generator 201, as described later on, defines a fraction f of period t_{CK} of clock CK. Signal CT together with signal SK define a corresponding timing, or transition edge in each sequence N that occurs, for example, once in each horizontal period H. The timing edge is shifted in time, by an amount that is determined in accordance with fraction f , relative to clock CK, and also relative to signal CT that occurs coincidentally with clock CK. Signal CT is also coupled to a decoder 23 that generates a signal MS having the period H that occurs coincidentally with clock CK. A pulse generator 54 generates, in accordance with signals SK and CT, a signal HORDRIVE, for example, once in each period H. Signal HORDRIVE provides the switching signal to a horizontal output stage 41 that operates at a frequency H that corresponds with that of signal HORDRIVE.

PLL 20 includes a phase detector 202, embodying an aspect of the invention. Phase detector 202 receives a signal 130. Signal 130 may be, for example, an analog, baseband, television signal that includes a signal portion that is referred to as synchronizing signal SYNC, occurring at the horizontal frequency f_H in each period H. Phase detector 202 also receives signals MS and SK that, together, define a timing or transition edge OSC of a periodic signal. Edge OSC is to be phase-compared in detector 202 with signal SYNC having a leading edge SY_{LE} . Phase detector 202 generates a phase difference signal PH (from microcomputer 140) in accordance with a difference between the instants when edges OSC and SY_{LE} occur,

respectively. Signal PH, that is analogous to an output signal of a phase detector of a conventional PLL, is used in PLL 20 for varying the phase of edge OSC to synchronize timing edge OSC to signal SYNC.

Signal PH is coupled via a low-pass-filter 33 that determines the response time of PLL 20. A filtered signal LPFO of filter 33 is coupled to an input terminal of a skew generator 201 that generates skew signals SK, that was mentioned before, and a signal PERIOD representative of the actual horizontal period H between sync pulses in integer number periods of clock CK. Signal PERIOD that is therefore also indicative of the period of sequence N is coupled to a comparator 200 that generates pulse RESET that resets counter 21, in accordance with signal PERIOD, for example, once in each period H.

During transient conditions, when timing edge OSC of PLL 20 is not yet in synchronism with signal SYNC, phase difference signal PH that is filtered in filter 33 varies the values of signals SK and CT in such a way to cause timing edge OSC to occur in synchronism with signal SYNC. The operation of a PLL that is similar to PLL 20 is described in detail in the Willis patent. It should be understood that phase detector 202, embodying the invention, operates differently from a corresponding phase detector of the PLL of the Willis patent.

FIGURES 2a-2g illustrate waveforms useful for explaining the operation of detector 202 of FIGURE 1. Similar symbols and numbers in FIGURES 1 and 2a-2g represent similar items or functions.

Analog baseband signal 130 of FIGURE 1 is coupled from, for example, a video detector of a television receiver, not shown in the FIGURES. Signal 130 is sampled, once in each period t_{CK} of a clock CK, by an analog-to-digital (A/D) converter 110 that produces a digitized signal 130a. When signal 130 is an NTSC type signal, the frequency of clock CK may be, for example, four times that of the color subcarrier.

Signal 130a is coupled via a digital lowpass filter 111 that generates from the samples of signal 130a a lowpass filtered signal 130b, shown schematically in FIGURE 2b. Lowpass filter 111 of FIGURE 1 reduces accompanying noise. Filter 111 also establishes a predetermined rate of change r' of a defined slope r between the corresponding values of consecutively occurring samples of the leading edge of signal 130b of FIGURE 2b. The leading edge of signal 130b corresponds with leading edge SY_{LE} of synchronizing signal SYNC that is included in signal 130 of FIGURE 1. As a result of the smoothing operation of lowpass filter 111, the rate of change r' of slope r in signal 130b of FIGURE 2b tends to remain substantially the same with variations in the slope of the leading edge SY_{LE} in composite video signal.

Signal 130b is coupled to a first input port of a comparator 112 that receives at a second input port a slice level signal SL that may be generated in a con-

ventionally designed slice level detector 113. Slice level signal SL may be, in a simplified arrangement, a constant signal; alternatively, it may be a dynamically variable signal that varies in accordance with the amplitude of signal 130.

As long as signal 130b of FIGURE 2b is, for example, more positive than slice level signal SL, a sync signal H_s of FIGURE 2c, developed at an output terminal of comparator 112 of FIGURE 1, is at a first, or FALSE state. Signal H_s being FALSE indicates the occurrence of the corresponding portion in signal 130b that is not used for providing synchronizing information such as, for example, the entire active video line portion of a given period H. On the other hand, when signal 130b of FIGURE 2b becomes less positive than slice level signal SL, that occurs after time T_{fs} of FIGURE 2c, the state of signal H_s is TRUE, indicating the occurrence of sync pulse information in signal 130 of FIGURE 1.

Signal H_s of FIGURE 1, having a leading edge that occurs at time T_{fs} of FIGURE 2c, occurs when signal 130b of FIGURE 1 becomes less positive than slice level signal SL. Thus, a value of a difference between signals 130b and SL changes polarity at time T_{fs} of FIGURE 2b. Signal H_s of FIGURE 1 is coupled, for example, to a conventionally built differentiator 121 that generates a pulse START of FIGURE 2g immediately following time T_{fs} . Pulse START is indicative of the occurrence of a corresponding level change in signal 130b of FIGURE 1.

Undelayed signal 130b and signal 130b that is delayed by one period t_{CK} of clock CK are coupled to input ports 125c and 125b, respectively, of a latch 125. Pulse START that is coupled to a clock receiving terminal 125a of latch 125 stores the corresponding signals at ports 125c and 125b at time T_{fs} of FIGURE 2b to provide output signals S_b and S_a of FIGURE 1, respectively.

Signal S_b provides the value of signal 130b of FIGURE 2b at time T_{fs} , when signal 130b is less positive than signal SL. Similarly, signal S_a provides the value of signal 130b of FIGURE 2b at the immediately preceding edge of clock t_{CK} at a time T_a , when signal 130b is more positive than signal SL.

At time T_a of FIGURE 2b, that occurs coincidentally with clock CK, and one period t_{CK} prior to time T_{fs} , the value of signal 130b that establishes signal S_a of FIGURE 1, is more positive than slice level signal SL of FIGURE 2b by an amount, referred to as "a". Similarly, at time T_{fs} , the value of signal 130b, that establishes signal S_b of FIGURE 1, is less positive than signal SL of FIGURE 2b by an amount, referred to as "b".

Pulse START is also coupled to a SET input terminal 115a of a RESET-SET (R-S) flip-flop 115, causing an output signal 115b to assume a TRUE state at an output Q terminal of flip-flop 115, that is coupled to an input 117a of an "AND" gate 117. The signal at output Q terminal being TRUE, enables "AND" gate

117 to couple the pulses of clock CK to a clock receiving input terminal 116a of a counter 116 that counts the pulses of clock CK. Pulse START is additionally coupled through an "OR" gate 118 to a RESET input terminal 116b of counter 116 for initializing an output signal COUNT of counter 116 to zero at the beginning of each computation cycle of microcomputer 140 that computes the value of a signal PH. Each computation cycle occurs when pulse START occurs.

Signal COUNT provides the state of counter 116 and is used to provide various time-out information as will be described below. Signal COUNT of counter 116, for example, increments once each time clock CK occurs from the initial value that is zero until signal COUNT reaches an upper limit of, for example, 64.

Signal COUNT is coupled to an input port of a decoder 141 that generates a triggering edge 141a when signal COUNT attains a predetermined value that represents a time-out interval of, for example, two microseconds. Triggering edge 141a is coupled to a triggering edge receiving input terminal of a flip-flop 142. Edge 141a causes flip-flop 142 to store the TRUE/FALSE state of signal H_s at the end of such time-out interval to form a signal VALID that is coupled to microcomputer 140.

In the event that signal H_s is FALSE at the end of the time-out interval, when edge 141a occurs, signal VALID becomes FALSE. This may result from a sync signal SYNC of signal 130 being narrower than the minimum requirement of two microseconds. On the other hand, if signal H_s is TRUE at the time edge 141a occurs, representing a sufficiently acceptable duration of sync signal SYNC, signal VALID becomes TRUE. Only when signal VALID is TRUE, will microcomputer 140 compute the value of phase difference signal PH, as described later on.

When signal COUNT has reached the upper limit that in this example is equal to 64, representing a time out interval of approximately 5 microseconds, a decoder 122 that receives signal COUNT generates a signal UPDATE that is coupled through "OR" gate 118 to terminal 116b of counter 116 for initializing counter 116 to zero again to restart the computation cycle of signal PH.

Signal COUNT is also coupled to an input port 123a of a latch 123 that stores the value of signal COUNT, referred to hereinafter as value y, when an edge MSa of oscillator signal MS of FIGURE 2e occurs. Thus, an output signal COUNT1 at an output port 123b of latch 123 of FIGURE 1 contains the value y of signal COUNT that occurs when edge MSa of oscillator signal OSC of FIGURE 2e occurs. Signal COUNT1 or value y is indicative of the time elapsed between the leading edge of pulse START, at time T_{fs} of FIGURE 2g, and edge MSa of edge OSC of FIGURE 2e that occurs at time T_1 .

Assume that in the embodiment of FIGURE 1 signal MS changes simultaneously with signal COUNT.

Therefore, the value y represents signal COUNT1 prior to the occurrence of signal MS. It follows that the length of interval $T_{16}-T_1$ is equal to $(y+1)$ multiplied by t_{CK} , as shown in FIGURE 2f.

Pulse START of FIGURE 1 is coupled to a reset input RS of latch 123 to cause signals COUNT1 and COUNT to be initialized to zero at the beginning of each computation cycle of signal PH.

The computation by microcomputer 140 of signal PH in a given computation cycle begins when counter 116 reaches the upper limit = 64, thereby generating signal UPDATE in decoder 122 which is then read by the microcomputer 140. For the purpose of explaining the computation algorithm of signal PH in microcomputer 140, assume that the period t_{CK} of clock CK is normalized and is equal to unity.

In its first step of the computation cycle, microcomputer 140 tests signal VALID. If signal VALID is FALSE, indicating that the duration of sync signal SYNC is narrower than, for example, the minimum required two microseconds, microcomputer 140 rejects the current signal SYNC and considers the signal as being invalid. Microcomputer 140 then begins testing again the output of decoder 122 for detecting signal UPDATE in the next computation cycle. If signal VALID is TRUE, microcomputer 140 proceeds to compute signal PH in the current computation cycle in a second step which tests signal COUNT1.

A first hypothetical situation exists if the value y of signal COUNT1 is different from zero. This situation exists when the phase difference is within a window period of, for example, approximately 5 microseconds that is determined by the upper count limit 64 of counter 116. In this situation, edge MSa of FIGURE 2e occurs before counter 116 of FIGURE 1 reaches its upper limit. As mentioned previously, counter 116 begins counting upon the occurrence of pulse START such as at time T_{16} of FIGURE 2d and ends counting approximately 5 microseconds later at a count of 64 clock periods at time T_{68} .

A simulated sync signal SIM of FIGURE 2d has a duration that corresponds with the window period. Signal SIM that represents a mathematical equivalent of sync signal 130b of FIGURE 1 is analytically reconstructed by microcomputer 140 from the samples of signal 130b by means of interpolation. Signal SIM of FIGURE 2d has a leading edge where the characteristic slope r of signal 130b of FIGURE 2b is computed to be equal to slice signal SL at a zero crossing time T_{20} that occurs between times T_a and T_{16} . Time T_{20} is calculated in microcomputer 140 by, for example, simple trigonometric interpolation from the values "a" and "b" of FIGURE 2b derived from signals S_a and S_b stored in latch 125 of FIGURE 1. Other conventional interpolation techniques may be used instead of the trigonometric one. The result of the computational interpolation is that crossover time T_{20} is computed to occur before time T_{16} by an interval X of FIGURE 2a,

where X is a fraction of clock period t_{CK} and is equal to $X = \left(\frac{b}{a+b}\right)xt_{CK}$.

Embodiment an aspect of the invention, time T_{20} of FIGURE 2d defines the time, to within a fraction of a clock period, when a leading edge occurs of simulated, or computed, sync signal SIM of FIGURE 2d. Signal SIM is derived from the synchronizing pulse in video signal 130 of FIGURE 1. Therefore, computation of phase difference signal PH of FIGURE 1 may be based on the use of simulated signal SIM to advantageously generate phase difference signal PH to within a fraction of a clock.

Embodiment an additional aspect of the invention, simulated sync signal SIM of FIGURE 2d, having a leading edge at time T_{20} , is defined as having a fixed rather than a variable width. The fixed width is selected to equal an integer k , such as, for example, $k=65$, multiplied by the length of period t_{CK} of clock CK of FIGURE 2a.

The value k determines a dynamic range or the window period of phase detector 202 of FIGURE 1. When the time difference between the input signal SYNC and edge OSC is smaller than approximately 5 microseconds, as determined by the width of signal SIM, a change in phase in edge SY_{LE} , for example, will cause a corresponding proportional change in signal PH. Outside the dynamic range, a change in phase will not produce any corresponding proportional change in signal PH. Thus outside the dynamic range signal PH may retain a constant value. Such characteristic of detector 202 is useful for obtaining a fast settling time in PLL 20 when a phase perturbation occurs in, for example, signal SYNC.

To provide for a width of $k=65$, the simulated trailing edge of simulated signal SIM of FIGURE 2d is defined to occur at a time T_6 . Time T_6 occurs after the lapse of an interval $\left(1 - \frac{b}{a+b}\right)$ clock periods t_{CK} following that edge of clock CK that is coincident with time T_{68} . Time T_{68} follows time T_{16} by $64xt_{CK}$ clock periods. During the interval $T_{20}-T_6$ of FIGURE 2d, simulated sync signal SIM is defined to be at a TRUE state.

Edge OSC of FIGURE 2e, that is to be phase compared with signal SIM of FIGURE 2d, includes signals MS and SK of FIGURE 1, as described before. Transition edge MSa of signal MS, that occurs at, for example, time T_1 , occurs coincidentally with a corresponding edge of periodic clock CK of FIGURE 2a. Also as described before, signal SK of FIGURE 1, that is referred to as a skew signal, is a digital word that represents the value of a fraction f of period t_{CK} of clock CK of FIGURE 2a. Taken together, signals MS and SK of FIGURE 1, define periodic timing edge OSC. Edge OSC is analogous to the output signal of a VCO of a conventional PLL. Edge OSC occurs at time T_2 of FIGURE 2e that occurs, for example, at time $T_2=T_1+ft_{CK}$. Time T_2 therefore occurs between

transition edge MSa and that of the next clock CK of FIGURE 2. Edge OSC is thus defined with a resolution that is better than period t_{CK} of FIGURE 2a.

Embodying a further aspect of the invention, periodic timing edge OSC of FIGURE 2e is phase compared in detector 202 of FIGURE 1 with simulated signal SIM of FIGURE 2d. Because simulated signal SIM of FIGURE 2d has a width that is equal to integer multiple k of period t_{CK} , the phase computation of signal PH, advantageously, remains correct even when both the duration of horizontal period H and the width of sync signal SYNC of video signal 130 of FIGURE 1 are not each equal to an integer multiple of period t_{CK} . The duration of the period H may vary when video signal 130 of FIGURE 1 is, for example, generated by a video tape recorder.

Advantageously, samples of signal 130b of FIGURE 2b that are not associated with leading edge SY_{LE} of FIGURE 1 are excluded from affecting the computation of signal PH. Since the information needed to construct simulated sync signal SIM is obtained from the sampled sync signal 130b only at times T_a and T_b of FIGURE 2b, any noise that is associated with signal 130b at other times, advantageously, does not significantly affect the accuracy of the computation of phase difference signal PH of FIGURE 1.

Embodying an aspect of the invention, phase difference signal PH is related to the time difference between the leading edge of simulated sync signal SIM of FIGURE 2d and transition edge OSC of FIGURE 2e, as defined by signals MS and SK of FIGURE 1. This difference is derived by microcomputer 140 by computing the difference between the length of interval T_2-T_{20} of FIGURES 2d-2g and the length of interval T_0-T_2 .

The length A_p in FIGURE 2f of interval T_2-T_{20} of FIGURE 2d is equal to the sum of three terms :

$\frac{b}{a+b}$, $y+1$ and fraction f . As explained before, the

term $\frac{b}{a+b}$ is equal to the length of interval X of FIG-

URE 2b, the value y is contained in signal COUNT1 of FIGURE 1, and fraction f is contained in skew word SK. The length A_n of FIGURE 2f of interval T_0-T_2 of FIGURE 2d is equal to the sum of three terms: $1-f$, $64-$

$y-2$ and $(1 - \frac{b}{a+b})$, as shown schematically in FIG-

URE 2f. Thus, signal PH of Figure 1 is equal to a difference A_p-A_n that is equal to $(\frac{2b}{a+b} + 2f) + (2y - 63)$.

The first parenthetical term may include a fraction of period t_{CK} . The second parenthetical term indicates an integer multiple of period t_{CK} .

The closer that edge OSC of FIGURE 2e is to time T_{20} , the more negative is signal PH of FIGURE 1. On the other hand, the closer that edge OSC of FIGURE 2e is to time T_0 , the more positive is signal

PH of FIGURE 1. Phase difference signal PH is zero when timing edge OSC of FIGURE 2e occurs at a predetermined instant relative to time T_{20} that is approximately at the center of interval $T_{20}-T_0$ of FIGURE 2d.

Embodying an aspect of the invention, phase difference signal PH is proportional to the time difference between time T_2 , corresponding to transition edge OSC of FIGURE 2e as defined by signals MS and SK of FIGURE 1, and time T_{20} of FIGURE 2d, determined by the leading transition edge of sync signal SYNC of signal 130 of FIGURE 1. To derive this time difference, microcomputer 140 of phase detector 202 uses synchronization information derived from simulated signal SIM having a leading transition edge that is determined by the leading edge of sync signal SYNC of signal 130 of FIGURE 1 and having a width that is equal to an integer multiple of clock period t_{CK} . The other information used is the oscillator timing information derived from skew signal SK, and from signal MS having edge MSa that occurs coincidentally with clock CK.

This concludes an explanation of the first hypothetical situation where oscillator edge OSC of FIGURE 2e occurs inside the window period, or interval $T_{20}-T_0$ of FIGURE 2d that is defined by simulated signal SIM. Such window period is established by signal SIM. The length of the window period is equal to, for example, approximately 5 microseconds, as described before.

In second and third hypothetical situations, that are described below, the phase difference is outside the window period that is established by signal SIM. In these situations, it may be desirable, to establish signal PH at a constant level in order to obtain a fast response or settling time of PLL 20 of FIGURE 1 when phase perturbation occurs. Such constant level of signal PH has a corresponding polarity that is indicative of a phase lag, when the second situation exists, or of a phase lead, when the third situation exists. Accordingly, pulse START is also coupled to a triggering terminal of a flip-flop 124 that stores the TRUE/FALSE state of signal MS of FIGURE 2d at time T_b to generate the corresponding TRUE/FALSE state of a signal POLARITY that is used for distinguishing between the second and third situations. The state of signal POLARITY of FIGURE 1 at an output terminal of flip-flop 124 provides microcomputer 140 with the state of signal MS at time T_b of FIGURE 2e. Signal POLARITY is used in the second and third hypothetical situations for determining whether the phase difference is positive or negative.

The second hypothetical situation exists when the phasing between sync signal SIM and oscillator edge OSC occurs after time T_0 of FIGURE 2e. In this situation, both the value y of signal COUNT1 of FIGURE 1 is zero and signal POLARITY, that is tested by microcomputer 140, is FALSE. This occurs, for example, when edge MSa' of signal MS and the corre-

sponding edge OSC of FIGURE 2e occur, after time T_0 , as shown by the corresponding dashed line in FIGURE 2e. In the second hypothetical situation microcomputer 140 of FIGURE 1 establishes signal PH to be at a constant predetermined positive value that is the same irrespective of the particular value of the phase difference.

A third hypothetical situation exists when the phasing between sync signal SIM and oscillator edge OSC is such that edge OSC occurs prior to time T_{z0} of FIGURE 2e. In this situation, both the value y is zero and signal POLARITY is TRUE. This occurs where edge MSa" of signal MS of FIGURE 2e occurs prior to time T_{z0} , as shown by the corresponding dashed line. In the third hypothetical situation, signal PH of FIGURE 1 is established by microcomputer 140 to be at a constant predetermined negative value that is the same irrespective of the particular value of the phase difference.

After the computation of signal PH is accomplished, microcomputer 140 begins testing for the next occurrence of signal UPDATE. When signal UPDATE is again detected after signal SYNC of the following period H is received, the computation cycle of signals PH begins again.

Claims

1. A digital phase detector responsive to first and second input signals for generating a phase difference signal that is indicative of a phase difference therebetween, comprising:
 - a source of a periodic clock signal;
 - sampling means (110) responsive to said first input signal (130) and to said clock signal (CK) for sampling said first input signal (130) to generate a sampled signal (130a) that contains first and second sampled values of said first input signal, each of said first and second sampled values being representative of said first input signal (130) at corresponding first and second instants that occur synchronously with respect to said clock signal (CK); characterized by
 - computing means (140) being responsive to said sampled signal (130a) for computing, by interpolation of said first and second sampled values, a third value that is representative of said first input signal (130) at a third instant when a transition edge (SY_{LE}) in said first input signal (130) is estimated to occur, said computing means (140) further being responsive to said second input signal for computing a difference between said third instant and a corresponding instant when a corresponding transition edge in said second input signal (OSC) occurs to generate said phase difference signal (PH) in accordance with said difference.
2. A phase detector according to Claim 1 characterized in that said computing means comprises a microcomputer (140).
3. A phase detector according to Claim 1 characterized in that said second input signal (OSC) comprises a first signal part (MS) that is synchronous with said clock signal (CK) and a second signal part (SK) containing a value that is indicative of a fraction of the period of said clock signal such that both said first (MS) and second (SK) parts in combination are indicative of said corresponding instant when said corresponding transition edge (SY_{LE}) occurs in said second input signal (130) to within a fractional period of said clock signal (CK).
4. A phase detector according to Claim 3 characterized in that said second signal part (SK) defines said corresponding instant relative to an instant that is defined by said first signal part (MS).
5. A phase detector according to Claim 3 characterized in that said computing means (140) generates said phase difference signal (PH) in accordance with a fourth instant separated from said third instant by an integer multiple of the period of said clock signal (CK).
6. A phase detector according to Claim 5 characterized in that said computing means (140) generates said phase difference signal (PH) at a predetermined value that remains unchanged when said corresponding transition edge in said second input signal (OSC) occurs outside an interval that is between said third and fourth instants.
7. A phase detector according to Claim 1 characterized in that said first input signal (130) is representative of a synchronizing pulse in a baseband video signal.
8. A phase detector according to Claim 1 characterized in that said first input signal (130) is at a television line rate.
9. A phase detector according to Claim 7 characterized by a comparator (112) responsive to a synchronizing pulse slice level signal (SL) and to said sampled signal (130a) for generating a third signal (H_S) when a difference therebetween changes polarity.
10. A phase detector according to Claim 9 characterized by means (125) responsive to said third signal (H_S) and to said sampled signal (130a) for selecting said first and second sampled values such that each of said first and second instants



sponding edge OSC of FIGURE 2e occur, after time T_{01} , as shown by the corresponding dashed line in FIGURE 2e. In the second hypothetical situation microcomputer 140 of FIGURE 1 establishes signal PH to be at a constant predetermined positive value that is the same irrespective of the particular value of the phase difference.

A third hypothetical situation exists when the phasing between sync signal SIM and oscillator edge OSC is such that edge OSC occurs prior to time T_{20} of FIGURE 2e. In this situation, both the value y is zero and signal POLARITY is TRUE. This occurs where edge MSa" of signal MS of FIGURE 2e occurs prior to time T_{20} , as shown by the corresponding dashed line. In the third hypothetical situation, signal PH of FIGURE 1 is established by microcomputer 140 to be at a constant predetermined negative value that is the same irrespective of the particular value of the phase difference.

After the computation of signal PH is accomplished, microcomputer 140 begins testing for the next occurrence of signal UPDATE. When signal UPDATE is again detected after signal SYNC of the following period H is received, the computation cycle of signals PH begins again.

Claims

1. A digital phase detector responsive to first and second input signals for generating a phase difference signal that is indicative of a phase difference therebetween, comprising:
 - a source of a periodic clock signal;
 - sampling means (110) responsive to said first input signal (130) and to said clock signal (CK) for sampling said first input signal (130) to generate a sampled signal (130a) that contains first and second sampled values of said first input signal, each of said first and second sampled values being representative of said first input signal (130) at corresponding first and second instants that occur synchronously with respect to said clock signal (CK); characterized by
 - computing means (140) being responsive to said sampled signal (130a) for computing, by interpolation of said first and second sampled values, a third value that is representative of said first input signal (130) at a third instant when a transition edge (SY_{LE}) in said first input signal (130) is estimated to occur, said computing means (140) further being responsive to said second input signal for computing a difference between said third instant and a corresponding instant when a corresponding transition edge in said second input signal (OSC) occurs to generate said phase difference signal (PH) in accordance with said difference.
2. A phase detector according to Claim 1 characterized in that said computing means comprises a microcomputer (140).
3. A phase detector according to Claim 1 characterized in that said second input signal (OSC) comprises a first signal part (MS) that is synchronous with said clock signal (CK) and a second signal part (SK) containing a value that is indicative of a fraction of the period of said clock signal such that both said first (MS) and second (SK) parts in combination are indicative of said corresponding instant when said corresponding transition edge (SY_{LE}) occurs in said second input signal (130) to within a fractional period of said clock signal (CK).
4. A phase detector according to Claim 3 characterized in that said second signal part (SK) defines said corresponding instant relative to an instant that is defined by said first signal part (MS).
5. A phase detector according to Claim 3 characterized in that said computing means (140) generates said phase difference signal (PH) in accordance with a fourth instant separated from said third instant by an integer multiple of the period of said clock signal (CK).
6. A phase detector according to Claim 5 characterized in that said computing means (140) generates said phase difference signal (PH) at a predetermined value that remains unchanged when said corresponding transition edge in said second input signal (OSC) occurs outside an interval that is between said third and fourth instants.
7. A phase detector according to Claim 1 characterized in that said first input signal (130) is representative of a synchronizing pulse in a baseband video signal.
8. A phase detector according to Claim 1 characterized in that said first input signal (130) is at a television line rate.
9. A phase detector according to Claim 7 characterized by a comparator (112) responsive to a synchronizing pulse slice level signal (SL) and to said sampled signal (130a) for generating a third signal (H_S) when a difference therebetween changes polarity.
10. A phase detector according to Claim 9 characterized by means (125) responsive to said third signal (H_S) and to said sampled signal (130a) for selecting said first and second sampled values such that each of said first and second instants



is determined relative to an instant when said third signal (H_s) is generated.

11. A phase detector according to Claim 10 characterized in that said computing means (140) is responsive to said third signal (H_s) for estimating said transition edge in said first input signal (130) to occur at said third instant that occurs prior to the generation of third signal (H_s) by an interval that is related to said first value divided by a sum of said first and second values. 5 10
12. A phase detector according to Claim 10 characterized in that said computing means (140) is responsive to said third signal (H_s) for estimating said transition edge in said first input signal (130) to occur at said third instant that is intermediate said first and second instants. 15
13. A phase detector according to Claim 1, for use in a television apparatus, characterized in that said first input signal is a baseband video signal (130), and said transition edge in said first input signal comprises the leading edge of a synchronizing pulse. 20
14. A digital phase detector responsive to a first input signal (130) having a pulse that includes first and second transition edges that change in opposite manner such that both said first and second transition edges define said pulse, and responsive to a second input signal (OSC) for generating a phase difference signal (PH) that is indicative of a phase difference between said first (130) and second (OSC) input signals, comprising: 25
 - a source of a periodic clock signal (CK);
 - sampling means (110) responsive to said first input signal (130) and to said clock signal (CK) for generating a sampled signal (130a) that contains a plurality of sample portions that are representative of corresponding levels in said first input signal (130); characterized by 30
 - second means (140) responsive to said sampled signal (130a) for selecting, from said plurality of sample portions, a first sample portion that is indicative of a first instant when said first transition edge occurs such that, in selecting said first sample portion, said second means (140) excludes each sample portion of said plurality of sample portions that corresponds to any portion of said pulse that is not associated with said first transition edge, said second means (140) being responsive to said second input signal (OSC) for generating said phase difference (PH) in accordance with said second input signal (OSC) and in accordance with said first sample portion to the exclusion of the remaining ones of said plurality of sample portions. 35 40 45 50
15. A phase detector according to Claim 14 characterized in that said second means (140) detects a change in said sampled signal that is indicative of the occurrence of said first transition edge and selects from said plurality of sample portions a second sample portion that corresponds to a portion of said first input signal that occurs prior to said first instant for generating said phase difference (PH) in accordance with said first and second sample portions. 55
16. A phase detector according to Claim 15 characterized in that said second means (140) generates in accordance with said first and second sample portions, using interpolation, a first value that is representative of said first instant such that said first instant occurs intermediate an instant that corresponds with said first sample portion and an instant that corresponds with said second sample portion.
17. A phase detector according to Claim 16 characterized in that the length of an interval between said instants that correspond with said first and second sample portions is equal to the period of said clock signal (CK).
18. A phase detector according to Claim 16 characterized in that said second means (140) generates in accordance with said first value a second value that is indicative of a time elapsed between said first instant and an instant that corresponds with a transition edge in said second input signal (OSC).
19. A phase detector according to Claim 14 characterized in that said second input signal (OSC) includes a first signal portion (MS) that represents a transition edge in said second input signal with a resolution that is in accordance with the period of said clock signal and a second signal portion (SK) that represents a skew of said transition edge relative to said first signal portion (MS) of said second input signal (OSC) with a resolution of a fraction of the period of said clock signal (CK).
20. A phase detector according to Claim 14 characterized in that said phase difference signal (PH) is capable of providing phase information that is required for controlling a horizontal phase-lock loop circuit (20) of a television apparatus.

Patentansprüche

1. Digital-Phasendetektor, der auf erste und zweite Eingangssignale zum Erzeugen eines Phasen-



Differenzsignals anspricht, das für eine Phasendifferenz zwischen ihnen kennzeichnend ist, enthaltend:

- eine Quelle eines periodischen Taktsignals;
- ein Abtastmittel (110), das auf das erste Eingangssignal (130) und das Taktsignal (CK) anspricht, zum Abtasten des ersten Eingangssignals (130), um ein abgetastetes Signal (130a) zu erzeugen, das erste und zweite Abtastwerte des ersten Eingangssignals enthält, wobei jede der ersten und zweiten Abtastwerte repräsentativ für das erste Eingangssignal (130) zu korrespondierenden ersten und zweiten Zeitpunkten ist, die synchron bezüglich des Taktsignals (CK) auftreten;

gekennzeichnet durch

- ein Berechnungsmittel (140), das auf das Abtastsignal (130a) anspricht, zum Berechnen eines dritten Wertes durch Interpolation aus den ersten und zweiten Abtastwerten, der repräsentativ für das erste Eingangssignal (130) zu einem dritten Zeitpunkt ist, zu dem geschätzt wird, daß eine Übergangsflanke (SY_{LE}) in dem ersten Eingangssignal (130) auftritt, wobei das Berechnungsmittel (140) weiter auf das zweite Eingangssignal anspricht zum Berechnen einer Differenz zwischen dem dritten Zeitpunkt und einem korrespondierenden Zeitpunkt, zu dem eine korrespondierende Übergangsflanke in dem zweiten Eingangssignal (OSC) auftritt, um das Phasendifferenz-Signal (PH) in Übereinstimmung mit der Differenz zu erzeugen.

2. Phasendetektor nach Anspruch 1, dadurch gekennzeichnet, daß das Berechnungsmittel einen Mikrocomputer (140) enthält.
3. Phasendetektor nach Anspruch 1, dadurch gekennzeichnet, daß das zweite Eingangssignal (OSC) einen ersten Signalteil (MS), der mit dem Taktsignal (CK) synchron ist und einen zweiten Signalteil (SK) enthält, der einen Wert beinhaltet, der kennzeichnend für einen Bruch bzw. Bruchteil der Periode des Taktsignals so ist, daß beide, der erste (MS) und der zweite (SK) Teil in Kombination - bis auf eine Bruchteils-Periode des Taktsignals (CK) - kennzeichnend für den korrespondierenden Zeitpunkt sind, wenn die korrespondierende Übergangsflanke (SY_{LE}) in dem zweiten Eingangssignal (130) auftritt.
4. Phasendetektor nach Anspruch 3, dadurch gekennzeichnet, daß der zweite Signalteil (SK) den korrespondierenden Zeitpunkt relativ zu einem Zeitpunkt defi-

niert, der von dem ersten Signalteil (MS) definiert wird.

5. Phasendetektor nach Anspruch 3, dadurch gekennzeichnet, daß das Berechnungsmittel (140) das Phasendifferenz-Signal (PH) in Übereinstimmung mit einem vierten Zeitpunkt erzeugt, der von dem dritten Zeitpunkt um ein ganzzahliges Vielfaches der Periode des Taktsignals (CK) beabstandet bzw. getrennt ist.
6. Phasendetektor nach Anspruch 5, dadurch gekennzeichnet, daß das Berechnungsmittel (140) das Phasendifferenz-Signal (PH) mit einem vorbestimmten Wert erzeugt, der unverändert bleibt, wenn die korrespondierende Übergangsflanke in dem zweiten Eingangssignal (OSC) außerhalb eines Intervalls auftritt, das zwischen dem dritten und vierten Zeitpunkt liegt.
7. Phasendetektor nach Anspruch 1, dadurch gekennzeichnet, daß das erste Eingangssignal (130) repräsentativ für einen Synchron-Impuls in einem Basisband-Video signal ist.
8. Phasendetektor nach Anspruch 1, dadurch gekennzeichnet, daß das erste Eingangssignal (130) mit einer Fernseh-Zeilenrate vorliegt.
9. Phasendetektor nach Anspruch 7, gekennzeichnet durch einen Komparator (112), der auf ein Synchronpuls-Trennpegel-Signal (SL) und auf das Abtastsignal (130a) zum Erzeugen eines dritten Signals (H_S) anspricht, wenn eine dazwischenliegende Differenz ihre Polarität ändert.
10. Phasendetektor nach Anspruch 9, gekennzeichnet durch ein Mittel (125), das auf das dritte Signal (H_S) und auf das abgetastete Signal (130a) zum Wählen des ersten und zweiten Abtastwertes so anspricht, daß jeder der ersten und zweiten Zeitpunkte relativ zu einem Zeitpunkt bestimmt ist, zu dem das dritte Signal (H_S) erzeugt wird.
11. Phasendetektor nach Anspruch 10, dadurch gekennzeichnet, daß das Berechnungsmittel (140) auf das dritte Signal (H_S) anspricht zum Schätzen des Auftretens der Übergangsflanke in dem ersten Signal (130) zu dem dritten Zeitpunkt der - um ein Intervall, das auf den ersten Wert geteilt durch eine Summe der ersten und zweiten Werte Bezug hat - vor der Erzeugung des dritten Signals (H_S) auftritt.



12. Phasendetektor nach Anspruch 10, dadurch gekennzeichnet, daß das Berechnungsmittel (140) auf das dritte Signal (H_3) anspricht zum Schätzen des Auftretens der Übergangsflanke in dem ersten Eingangssignal (130) zu dem dritten Zeitpunkt, der zwischen dem ersten und zweiten Zeitpunkt liegt. 5
13. Phasendetektor nach Anspruch 1 zur Verwendung in einer Fernscheinrichtung, dadurch gekennzeichnet, daß das erste Eingangssignal ein Basisband-Videosignal (130) ist und die Übergangsflanke in dem ersten Eingangssignal die Vorderflanke eines Synchron-Impulses beinhaltet. 10
14. Digital-Phasendetektor, der auf ein erstes Eingangssignal (130) und ein zweites Eingangssignal (OSC) anspricht, wobei ersteres einen Impuls mit erster und zweiter Übergangsflanke umfaßt, die entgegengesetzt gerichtet sind, so daß beide, die erste und zweite Übergangsflanke, den Impuls definieren, zum Erzeugen eines Phasendifferenz-Signals (PH), das für eine Phasendifferenz zwischen dem ersten (130) und zweiten (OSC) Eingangssignal kennzeichnend ist, enthaltend: 15
- eine Quelle eines periodischen Taktsignals (CK);
 - ein Abtastmittel (110), das auf das erste Eingangssignal (130) und das Taktsignal (CK) anspricht, zum Erzeugen eines abgetasteten Signals (130a), das mehrere Abtastteile beinhaltet, die repräsentativ für korrespondierende Pegel in dem ersten Eingangssignal (130) sind; gekennzeichnet durch 20
 - ein zweites Mittel (140), das auf das abgetastete Signal (130a) anspricht, zum Wählen eines ersten Abtastteils aus den mehreren Abtastteilen, der kennzeichnend für einen ersten Zeitpunkt ist, zu dem die erste Übergangsflanke auftritt, so daß durch Wählen des ersten Abtastteils das zweite Mittel (140) jeden Abtastteil der mehreren Abtastteile, der mit jedem (anderen) Teil/Abschnitt des Impulses korrespondiert, der nicht der ersten Übergangsflanke zugeordnet ist, ausschließt, wobei das zweite Abtastmittel (140) auf das zweite Eingangssignal (OSC) anspricht zum Erzeugen der Phasendifferenz (PH) in Übereinstimmung mit dem zweiten Eingangssignal (OSC) und in Übereinstimmung mit dem ersten Abtastteil, wobei die verbleibenden Teile der mehreren Abtastteile ausgeschlossen werden. 25
15. Phasendetektor nach Anspruch 14, dadurch gekennzeichnet, daß das zweite Mittel (140) eine Änderung in dem abgetasteten Signal erfaßt, die kennzeichnend für das Auftreten der ersten Übergangsflanke ist und aus der Mehrzahl der Abtastteile einen zweiten Abtastteil auswählt, der mit einem Teil des ersten Eingangssignals korrespondiert, der vor dem ersten Zeitpunkt liegt, zur Erzeugung der Phasendifferenz (PH) in Übereinstimmung mit dem ersten und zweiten Abtastteil (sample portion). 30
16. Phasendetektor nach Anspruch 15, dadurch gekennzeichnet, daß das zweite Mittel (140) in Übereinstimmung mit dem ersten und zweiten Abtastteil unter Verwendung von Interpolation einen - für den ersten Zeitpunkt repräsentativen - ersten Wert erzeugt, so daß der erste Zeitpunkt zwischen einem Zeitpunkt, der mit dem ersten Abtastteil korrespondiert, und einem Zeitpunkt, der mit dem zweiten Abtastteil korrespondiert, auftritt. 35
17. Phasendetektor nach Anspruch 16, dadurch gekennzeichnet, daß die Länge eines Intervalls zwischen den Zeitpunkten, die mit den ersten und zweiten Abtastteilen korrespondieren, gleich der Periode des Taktsignals (CK) ist. 40
18. Phasendetektor nach Anspruch 16, dadurch gekennzeichnet, daß das zweite Mittel (140) in Übereinstimmung mit dem ersten Wert einen zweiten Wert erzeugt, der kennzeichnend für eine verstrichene Zeit zwischen dem ersten Zeitpunkt und einem Zeitpunkt ist, der mit einer Übergangsflanke in dem zweiten Eingangssignal (OSC) korrespondiert. 45
19. Phasendetektor nach Anspruch 14, dadurch gekennzeichnet, daß das zweite Eingangssignal (OSC) einen ersten Signaltteil (MS), der eine Übergangsflanke in dem zweiten Eingangssignal mit einer Auflösung repräsentiert, die in Übereinstimmung mit der Periode des Taktsignals ist, und einen zweiten Signaltteil (SK) beinhaltet, der eine Verschiebung der Übergangsflanke relativ zu dem ersten Signaltteil (MS) des zweiten Eingangssignals (OSC) mit einer Auflösung eines Bruchteils der Periode des Taktsignals (CK) repräsentiert. 50
20. Phasendetektor nach Anspruch 14, dadurch gekennzeichnet, daß das Phasendifferenz-Signal (PH) in der Lage ist, Phaseninformation zur Verfügung zu stellen, die zum Steuern einer Horizontal-PLL-Schal- 55



tung (20) eines Fernsehgerätes benötigt wird.

Revendications

1. Détecteur de phase numérique sensible à des premier et second signaux d'entrée pour générer un signal de différence de phase qui est indicateur d'une différence de phase entre eux, comprenant :

une source d'un signal d'horloge périodique ;

un moyen d'échantillonnage (110) sensible audit premier signal d'entrée (130) et audit signal d'horloge (CK) pour échantillonner ledit premier signal d'entrée (130) pour générer un signal échantillonné (130a) qui contient des première et seconde valeurs échantillonnées dudit premier signal d'entrée, chacune desdites première et seconde valeurs échantillonnées étant représentatives dudit premier signal d'entrée (130) au niveau des premier et second instants correspondants qui se produisent de façon synchrone par rapport audit signal d'horloge (CK) ; caractérisé par

un moyen de calcul (140) sensible audit signal échantillonné (130a) pour calculer, par interpolation desdites première et seconde valeurs échantillonnées une troisième valeur qui est représentative du type du premier signal d'entrée (130) au niveau d'un troisième instant lorsqu'un bord de transition (SY_{LE}) dudit premier signal d'entrée (130) est estimé se produire, ledit moyen de calcul (140) étant, de plus, sensible audit second signal d'entrée pour calculer une différence entre ledit troisième instant et un instant correspondant à ce qu'un bord de transition correspondant dudit second signal d'entrée (OSC) se produise pour générer ledit signal de différence de phase (PH) en conformité avec ladite différence.

2. Détecteur de phase selon la revendication 1, caractérisé en ce que ledit moyen de calcul comprend un microcalculateur (140).
3. Détecteur de phase selon la revendication 1, caractérisé en ce que ledit second signal d'entrée (OSC) comprend une première partie de signal (MS) qui est synchrone audit signal d'horloge (CK) et une seconde partie de signal (SK) contenant une valeur qui est indicatrice d'une fraction de la période dudit signal d'horloge de telle sorte que les deux dites première (MS) et seconde (SK) parties en combinaison sont indicatrices dudit instant correspondant lorsque ledit bord de transition correspondant (SY_{LE}) se produit dans ledit second signal d'entrée (130) à l'intérieur d'une

période fractionnaire dudit signal d'horloge (CK).

4. Détecteur de phase selon la revendication 3, caractérisé en ce que ladite seconde partie de signal (SK) définit ledit instant correspondant relativement à un instant qui est défini par ladite première partie du signal (MS).
5. Détecteur de phase selon la revendication 3, caractérisé en ce que ledit moyen de calcul (140) génère ledit signal de différence de phase (PH) en conformité avec un quatrième instant séparé dudit troisième instant d'un multiple entier de période dudit signal d'horloge (CK).
6. Détecteur de phase selon la revendication 5, caractérisé en ce que ledit moyen de calcul (140) génère ledit signal de différence de phase (PH) au niveau d'une valeur prédéterminée qui reste inchangée lorsque ledit bord de transition correspondant dudit second signal d'entrée (OSC) se produit à l'extérieur d'un intervalle qui est situé entre lesdits troisième et quatrième instants.
7. Détecteur de phase selon la revendication 1, caractérisé en ce que ledit premier signal d'entrée (130) est représentatif d'une impulsion de synchronisation d'un signal vidéo en bande de base.
8. Détecteur de phase selon la revendication 1, caractérisé en ce que ledit premier signal d'entrée (130) est à une fréquence de ligne de télévision.
9. Détecteur de phase selon la revendication 7, caractérisé par un comparateur (112) sensible à un signal de seuil de comparaison d'impulsion de synchronisation (SL) et audit signal échantillonné (130a) pour générer un troisième signal (HS) lorsqu'une différence entre ces signaux change de polarité.
10. Détecteur de phase selon la revendication 9, caractérisé par un moyen (125) sensible audit troisième signal (H_S) et audit signal échantillonné (130a) pour sélectionner lesdites première et seconde valeurs échantillonnées de telle sorte que chacun desdits premier et second instants est déterminé relativement à un instant auquel ledit troisième signal (H_S) est produit.
11. Détecteur de phase selon la revendication 10, caractérisé en ce que ledit moyen de calcul (140) est sensible audit troisième signal (H_S) pour estimer que se produit ledit bord de transition dudit premier signal d'entrée (130) au niveau dudit troisième instant qui arrive avant la production du troisième signal (H_S) selon un intervalle qui est relié à ladite première valeur divisée par une som-



me desdites première et seconde valeurs.

12. Détecteur de phase selon la revendication 10, caractérisé en ce que ledit moyen de calcul (140) est sensible audit troisième signal (H_s) pour estimer que se produit ledit bord de transition dudit premier signal d'entrée (130) au niveau dudit troisième instant qui est situé entre lesdits premiers et seconds instants. 5
13. Détecteur de phase selon la revendication 1, pour utilisation dans un appareil de télévision, caractérisé en ce que ledit premier signal d'entrée est un signal vidéo en bande de base (130), et ledit bord de transition dudit premier signal d'entrée comprend le bord avant d'une impulsion de synchronisation. 10
14. Détecteur de phase numérique sensible à un premier signal d'entrée (130) comportant une impulsion qui comprend des premier et second bords de transition qui varient de façon opposée de telle sorte que les deux dits premier et second bords de transition définissent ladite impulsion, et sont sensibles à un second signal d'entrée (OSC) pour générer un signal de différence de phase (PH) qui est indicateur d'une différence de phase entre lesdits premier (130) et second (OSC) signaux d'entrée, comprenant : 15
 - une source d'un signal d'horloge périodique (CK); 20
 - un moyen d'échantillonnage (110) sensible audit premier signal d'entrée (130) et audit signal d'horloge (CK) pour générer un signal échantillonné (130a) qui contient une pluralité de parties d'échantillon qui est représentative des niveaux correspondants dudit premier signal d'entrée (130); caractérisé par 25
 - un second moyen (140) sensible audit signal échantillonné (130a) pour sélectionner à partir de ladite pluralité des parties d'échantillon, une première partie d'échantillon qui est indicatrice d'un premier instant auquel ledit premier bord de transition se produit de telle sorte que, en sélectionnant ladite première partie d'échantillon, ledit second moyen (140) exclut chaque partie d'échantillon de ladite pluralité des parties d'échantillon qui correspond à une partie quelconque de ladite impulsion qui n'est pas associée audit premier bord de transition, ledit second moyen (140) étant sensible audit second signal d'entrée (OSC) pour générer ledit signal de différence de phase (PH) en conformité avec ledit second signal d'entrée (OSC) et en conformité avec ladite première partie d'échantillon à l'exclusion des parties restantes de ladite pluralité des parties d'échantillon. 30
15. Détecteur de phase selon la revendication 14, caractérisé en ce que ledit second moyen (140) détecte une variation dudit signal échantillonné qui est indicatrice de l'occurrence dudit premier bord de transition et sélectionne à partir de ladite pluralité des parties d'échantillon une seconde partie d'échantillon qui correspond à une partie dudit premier signal d'entrée qui se produit avant ledit premier instant pour générer ladite différence de phase (PH) en conformité avec lesdites première et seconde parties d'échantillon. 35
16. Détecteur de phase selon la revendication 15, caractérisé en ce que ledit second moyen (140) génère en conformité avec lesdites première et seconde parties d'échantillon, en utilisant une interpolation, une première valeur qui est représentative dudit premier instant de telle sorte que ledit premier instant se produise entre un instant qui correspond à ladite première partie d'échantillon et un instant qui correspond à ladite seconde partie d'échantillon. 40
17. Détecteur de phase selon la revendication 16, caractérisé en ce que la longueur d'un intervalle entre lesdits instants qui correspondent auxdites première et seconde parties d'échantillon est égale à la période dudit signal d'horloge (CK). 45
18. Détecteur de phase selon la revendication 16, caractérisé en ce que ledit second moyen (140) génère, en conformité avec la première valeur, une seconde valeur qui est indicatrice d'un temps écoulé entre ledit premier instant et un instant qui correspond à un bord de transition dudit second signal d'entrée (OSC). 50
19. Détecteur de phase selon la revendication 14, caractérisé en ce que ledit second signal d'entrée (OSC) comprend une première partie de signal (MS) qui représente un bord de transition dudit second signal d'entrée ayant une résolution qui est en conformité avec la période dudit signal d'horloge et une seconde partie de signal (SK) qui représente un décalage dudit bord de transition relativement à ladite première partie de signal (MS) dudit second signal d'entrée (OSC) ayant une résolution d'une fraction de période dudit signal d'horloge (CK). 55
20. Détecteur de phase selon la revendication 14, caractérisé en ce que ledit signal de différence de phase (PH) est capable de fournir une information de phase qui est requise pour commander un circuit horizontal de boucle à verrouillage de phase (20) d'un appareil de télévision.