

- the exposure to the neutral or reducing atmosphere is carried out for a length of time comprised between 5 minutes and 5 hours.
- 5 - the thickness profile of the dielectric layer of the intermediate structure and the dissolution profile have a circular symmetry of axis perpendicular to the plane of the structure and passing through its centre.
- 10 According to an aspect of the invention, there is provided a process for fabricating a final structure comprising in succession a semiconductor layer having a thickness less than 100 nm, a buried dielectric layer and a carrier substrate, the process comprising: providing an
- 15 intermediate structure including an upper semiconductor layer, the buried dielectric layer and the carrier substrate; and finishing the intermediate structure to form the final structure by performing a smoothing anneal on the intermediate structure and nonuniformly modifying, by way
- 20 of a dissolution effect, a thickness of the buried dielectric layer following a predetermined dissolution profile; wherein the buried dielectric layer of the intermediate structure has a thickness profile complementary to the predetermined dissolution profile so
- 25 as to compensate for the non-uniform modification of the thickness of the buried dielectric layer.

BRIEF DESCRIPTION OF THE DRAWINGS

30 The invention will be better understood in light of the following description of one particular nonlimiting embodiment of the invention given with reference to the appended figures, in which:

- Figure 1 shows an intermediate and final structure obtained according to a prior-art process;
- 5 - Figure 2 shows the steps of the process of one particular embodiment of the present invention; and
- Figure 3 shows an exemplary dissolution profile.

10

DETAILED DESCRIPTION OF THE INVENTION

15

The process according to the invention is generally applicable to the fabrication of a final structure comprising a useful semiconductor layer, a dielectric layer and a carrier substrate.

20

With reference to Figure 2a, the process comprises providing an intermediate structure 1 comprising in succession an upper semiconductor layer 3, a dielectric layer 2, and a carrier substrate 4. This intermediate

CLAIMS

1. A process for fabricating a final structure comprising in succession a semiconductor layer having a thickness less than 100 nm, a buried dielectric layer and a carrier substrate, the process comprising:

providing an intermediate structure including an upper

semiconductor layer, the buried dielectric layer and the carrier substrate; and

finishing the intermediate structure to form the final structure by performing a smoothing anneal on the intermediate structure and nonuniformly modifying, by way of a dissolution effect, a thickness of the buried dielectric layer following a predetermined dissolution profile;

wherein the buried dielectric layer of the intermediate structure has a thickness profile complementary to the predetermined dissolution profile so as to compensate for the non-uniform modification of the thickness of the buried dielectric layer.

2. The process of claim 1, wherein the semiconductor layer comprises silicon and the dielectric layer comprises silicon oxide.

3. The process of claim 2, wherein the carrier substrate comprises a silicon substrate.

4. The process of claim 3, wherein the dielectric layer of the final structure has an average thickness smaller than or equal to 50 nm.

5. The process of claim 4, wherein the dielectric layer of the final structure has an average thickness in a range extending from 10 nm to 25 nm.

6. The process of claim 4, wherein providing the intermediate structure comprises:
forming a dielectric layer on a donor substrate;
forming a weak plane in the donor substrate defining a layer to be removed from the donor substrate between the weak plane and a surface of the donor substrate;
assembling a face of the donor substrate with the carrier substrate; and
detaching the layer to be removed from the donor substrate in order to remove the layer from the donor substrate and add the layer to the carrier substrate, the layer forming the upper semiconductor layer of the intermediate structure.

7. The process of claim 6, wherein finishing the intermediate structure further comprises thinning the upper semiconductor layer by sacrificial oxidation in order to form the semiconductor layer.

8. The process of claim 7, wherein finishing the intermediate structure further comprises annealing the intermediate structure to increase a bond strength between the upper semiconductor layer and the carrier substrate.

9. The process of claim 8, wherein nonuniformly modifying the thickness of the dielectric layer comprises exposing the semiconductor layer or the upper semiconductor layer to a neutral or reducing atmosphere at a temperature of between 1,150°C. and 1,200°C.

10. The process of claim 9, wherein the exposure to the neutral or reducing atmosphere is carried out for a length of time of between 5 minutes and 5 hours.

11. The process of claim 10, wherein the thickness profile of the dielectric layer of the intermediate structure and the dissolution profile have a circular symmetry of axis perpendicular to the plane of the structure and passing through a center of the structure.

12. The process of claim 1, wherein the carrier substrate comprises a silicon substrate.

13. The process of claim 1, wherein the dielectric layer of the final structure has an average thickness smaller than or equal to 50 nm.

14. The process of claim 13, wherein the dielectric layer of the final structure has an average thickness in a range extending from 10 nm to 25 nm.

15. The process of claim 1, wherein providing the intermediate structure comprises:
forming a dielectric layer on a donor substrate;
forming a weak plane in the donor substrate defining a layer to be removed from the donor substrate between the weak plane and a surface of the donor substrate;
assembling a face of the donor substrate with the carrier substrate; and

detaching the layer to be removed from the donor substrate in order to remove the layer from the donor substrate and add the layer to the carrier substrate, the layer forming the upper semiconductor layer of the intermediate structure.

16. The process of claim 1, wherein finishing the intermediate structure further comprises thinning the upper semiconductor layer by sacrificial oxidation in order to form the semiconductor layer.

17. The process of claim 1, wherein finishing the intermediate structure further comprises annealing the intermediate structure to increase a bond strength between the upper semiconductor layer and the carrier substrate.

18. The process of claim 1, wherein nonuniformly modifying the thickness of the dielectric layer comprises exposing the semiconductor layer or the upper semiconductor layer to a neutral or reducing atmosphere at a temperature of between 1,150°C. and 1,200°C.

19. The process of claim 18, wherein the exposure to the neutral or reducing atmosphere is carried out for a length of time of between 5 minutes and 5 hours.

20. The process of claim 1, wherein the thickness profile of the dielectric layer of the intermediate structure and the dissolution profile have a circular symmetry of axis perpendicular to the plane of the structure and passing through a center of the structure.