Claims:

1. An apparatus for use in wafer package processing, comprising:

a substrate;

a plurality of die cavities formed through the substrate; and

a plurality of conductive through vias disposed through the substrate and arranged about the perimeter of each die cavity,

wherein a top surface of the substrate is exposed for application of an encapsulating layer and a bottom surface of the substrate is exposed for placement on an adhesive layer.

2. The substrate of claim 1, wherein the substrate is a printed circuit board.

3. The substrate of claim 1, wherein the substrate is a glass wafer.

4. The substrate of claim 1, wherein the plurality of conductive through vias are filled with one of copper or solder.

5. An electronics package comprising:

a substrate consisting of an array of die cavities formed in the substrate, wherein each die cavity is surrounded by one or more rows of through vias having conductive materials disposed therein;

a plurality of dies disposed in a cavity in the array of die cavities;

an encapsulating material disposed on the top surface of the substrate for securing the plurality of dies in place in each cavity in the substrate; and

a top redistribution layer abutting the encapsulating material, coupling the plurality of dies with the one or more rows of through vias, configured to couple with a top electronics packages stacked above the electronics package; and

a bottom redistribution layer abutting the encapsulating material, coupling the plurality of dies with the one or more rows of through vias, configured to couple with a bottom electronics packages stacked below the electronics package.

6. The electronics package of claim 5, wherein each via in the one or more rows of through vias are filled with Copper or solder.

7. The electronics package of claim 5, wherein the encapsulating material comprises an epoxy molding compound.

8. The electronics package of claim 5, wherein the array of die cavities is formed by an arrangement of one or more continuous strips of die cavities.

9. The electronics package of claim 5, wherein the array of die cavities is formed by an arrangement of individual die cavities.

10. The electronics package of claim 5, wherein the substrate is a printed circuit board.

11. The electronics package of claim 5, wherein the array of die cavities is formed in a glass substrate, and wherein the encapsulating material encapsulates the glass substrate and secures the plurality of dies in the glass substrate.

12. A method for wafer level packaging, comprising:

depositing an adhesive layer atop a carrier;

placing at least a portion of a substrate pre-fabricated with a plurality of die cavities disposed through the substrate and a plurality of conductive through vias disposed through the substrate atop the adhesive layer;

inserting a die into each of the die cavities forming an electronics package;

encapsulating the die and the substrate in an encapsulating material; and

debonding and removing the adhesive layer and the carrier from the encapsulated die and substrate.

13. The method of claim 12, wherein the adhesive layer is a molding tape.

14. The method of claim 12, wherein encapsulating the die and the substrate comprises a thermal compression molding process.

15. The method of claim 12, wherein the process temperature for encapsulating the electronics package is higher than the melting point temperature of the adhesive layer.

16. The method of claim 12, wherein the substrate is a printed circuit board (PCB).

17. The method of claim 16, further comprising:

slicing the PCB into smaller dimensions prior to placing the substrate atop the adhesive layer.

18. The method of claim 17, wherein the smaller dimensions comprise a single column of one or more contiguous die enclosures, the die enclosures comprising a cavity with a plurality of through vias arranged along the perimeter of the cavity in one or more rows.

19. The method of claim 12, wherein the substrate is a wafer and the entire wafer is placed on the adhesive layer.

20. The method of claim 19, wherein the wafer is a glass wafer.