

SERIAL-ACCESSED MEMORY DATA ACCESSING CIRCUIT INVOLVING LOW
OPERATING CURRENT, AND METHOD THEREOF

The present invention relates to a Serial-Accessed Memory (hereinafter referred to as SAM) data accessing circuit involving a low operating current and a method thereof, and particularly to a SAM data accessing circuit and a method thereof, in which the peak current can be reduced by separating the data sensing time and the data outputting time from each other, and the operating current can be reduced by preventing the consumption of the unnecessary current during the serial accessing.

Generally, in a dual port DRAM, a first port has the same structure as that of the normal DRAM, and a second port consists of a serial data register and a circuit for inputting/outputting the data in a serial manner.

Unlike the normal DRAM, such a dual port DRAM is capable of outputting the data in an independent manner, and the data accessing is carried out through the dual port, with the result that the power consumption becomes seriously high compared with the normal DRAM.

Therefore, if the dual port DRAM is to be kept from giving a serious problem in relation to the power consumption compared with the normal DRAM, then it is necessary that the data accessing be carried out with a minimum power consumption.

An object of the present invention is to provide a SAM data accessing circuit and a method thereof, in which the power consumption can be reduced by separating the data sensing time and the data outputting time.

According to one aspect of the present invention there is provided a SAM data accessing method involving a low operating current in accessing the data which is supplied from a RAM port memory array through a transmission gate to a SAM port memory array to be stored therein, wherein at the falling edge of a serial counting clock signal, i.e., at one and half cycles before the outputting of the data, the data is sensed from said SAM memory array so as for the data to be stored in a first section of a pipeline type two-section buffer;

at the falling edge of the serial counting clock signal, i.e., at half cycles before the outputting of the data, the data stored in said first section of said two-section buffer is transferred to a second section of said two-section buffer to be stored therein; and

at the rising edge of the serial counting clock signal, the data stored in a second section of said two-section buffer is outputted.

According to a further aspect of the invention there is provided a SAM data accessing circuit involving a low operating current, comprising: a serial counter for outputting a serial address by counting serial counting clock signals; column decoders for selecting an input/output gate; an input/output sense-amplifier for amplifying the data supplied through said input/output gate and an input/output line; a data outputting buffer for supplying to an input/output path the data amplified by said input/output sense-amplifier; a column predecoder for outputting a column decoder selecting signal after receipt of a serial address from said serial counter; a

serial decoding disabling circuit for outputting an enabling signal to said column predecoder after receipt of a serial counting clock signal, and for outputting a disabling signal to said column predecoder after receipt of a tracking signal from a tracking circuit; and a tracking circuit for outputting a tracking signal after receipt of a serial counting clock signal in order to control said input/output sense-amplifier by forming a layout in the same form as that of the layout of the signal path between the inputting of a serial counting clock signal and the supplying of the data from a SAM port memory array to said input/output sense-amplifier; wherein a pipeline type two-section buffer is adapted to store in a first section data sensed from the input/output line one and a half periods before supplying data to the input/output path, to transmit the data from the first section to a second section half a period before supplying data to the input/output path, and to output the data from the second section at a rising edge of the serial counting clock signal.

Embodiments of the present invention will now be described, by way of example with reference to the accompanying drawings, in which:

Figure 1A is a timing chart showing the outputting of data after carrying out a serial accessing to the data of SAM according to the conventional technique;

Figure 1B is a timing chart showing the outputting of the data after carrying out a serial accessing to the SAM data in an improved manner according to an embodiment of the present invention;

Figure 2 illustrates the current values measured during the SAM data accessing and outputting according to the conventional technique and according to an embodiment of the present invention in a comparative form;

Figure 3 is a block diagram of a SAM data accessing circuit of an embodiment of the present invention involving low operating current;

Figure 4 is a timing chart showing the accessing and outputting of the SAM data involving a low operating current according to an embodiment of the present invention;

Figures 5 to 7 are detailed circuit illustrations of the tracking circuit, the serial decoding disabling circuit and the column predecoder of Figure 3; and

Figure 8 is a detailed circuit illustration for an I/O sense-amplifier and an outputting buffer.

Figure 1 illustrates timing charts showing the data sensing time and the data outputting time in a dual port DRAM.

Conventionally, as shown in Figure 1A, the data is sensed and at the same time outputted at the rising edge of a serial counting clock signal SC, and therefore, at the portion where the data sensing operation and the data outputting operation are overlapped, i.e., at the rising edge of the clock signal SC, the peak currents are overlapped as shown in Figure 2 by the solid line, thereby problematically increasing the peak current.

The present invention is for preventing the increase of the peak currents caused by the simultaneous occurrence of the sensing operation and the outputting operation. As shown in Figure 1B, a data S1 to be outputted is accessed and sense-amplified in advance at $3/2$ cycles before the outputting, i.e., at the falling edge of the clock SC, and then, the data is stored in a first section of a two-section buffer by a pipeline method.

Thereafter, at the rising edge of the clock SC, the data D0 which is stored in a second section of the pipeline buffer after being sensed before one and half cycles is outputted.

Then, at the falling edge of the clock SC, a new data

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S2 is sensed, amplified and supplied to the first section of the pipeline type buffer, and the data S1 stored in the first section is transferred to the second section, while, upon arriving to another rising edge, the data S1 which has been stored in the second section is outputted as a data D1.

Thus, for these embodiments of the present invention, the sensing time and the outputting time for the serial data are different from each other, and therefore, as shown by solid lines in Figure 2, the peak currents are dispersed, thereby obtaining a power consumption decreasing effect.

As described above, the present invention is directed to decreasing the power consumption by separating the data sensing operation and the data outputting operation, and the present invention will be described in a further detail referring to Figures 3 and 4.

Figure 3 illustrates a circuit for serially accessing the data of the dual port memory according to an embodiment of the present invention. Here, reference code 1 indicates a RAM port memory array, and 2 indicates a SAM port array.

The SAM data accessing circuit comprises: a serial counter 3 for outputting a serial address SADDRi after receipt of a serial counting clock signal SC;

a column predecoder 4 for outputting a serial address PSAi to column decoders 5₁-5_N after decoding the serial address SADDRi supplied from the serial counter 3;

column decoders 5₁-5_N for outputting signals for gating an input/output gate (to be called hereinafter I/O gate) after receipt of an address PSAi from the column predecoder 4;

a tracking circuit for outputting track signals TRACK to an I/O sense-amplifier 8, to the column predecoder 4 and to a serial decoding disabling circuit 6, by timing by use of an equivalent circuit path the time until the column predecoder 4 predecodes the output of the serial counter SC starting from the falling edge of the serial counting clock signal SC, until the column decoders 5_1-5_N receive the output signals of the column predecoder 4 so as for an I/O gate to be selected, and until the data stored in the SAM port memory 2 is supplied from the RAM port memory array 1 through an I/O line to an I/O sense-amplifier 8;

a serial decoding disabling circuit 6 for outputting a serial decoding disabling signal to the column predecoder 4 after receipt of a serial counting clock signal SC, and for outputting a serial decoding disabling signal SDD to the column predecoder 4 after receipt of a tracking signal TRACK from the tracking circuit;

an I/O sense-amplifier 8 for amplifying the data supplied from the SAM port array 2 through an I/O gate and an I/O line selected by the column decoder 5_1-5_N ; and

a data outputting buffer 9 for outputting to an input/output buffer 10 the data amplified by the sense-amplifier.

Here, if the output data of a row selected from the RAM port memory array 1 consists of N bits, then the number of the required column lines is N.

Now the operation of accessing to the data according to an embodiment of the present invention will be described referring to the timing charts of Figure 4. If the data of the

RAM port memory array is to be serially accessed, then the data of one row of the RAM port memory array has to be sensed, and the sensed data has to be transferred through a transferring gate to the SAM port memory array 2 in advance.

— If a serial-counting clock signal SC is supplied from an external controller to the serial counter 3, then the serial counter 3 sequentially generates serial address signals in order to cause sequential generations of signals for selecting one of column lines in accordance with the clock signal SC.

As shown in Figure 4, when the signal SC is at the falling edge, the serial counter 3 is activated after a time interval t_1 , and supplies a serial address signal SADDRi of Figure 4B to the column predecoder 4. At the same time, the serial decoding disabling circuit 6 outputs a serial decoding disabling signal SDD (refer to the timing chart of Figure 4C) to the column predecoder 4, and therefore, the column predecoder 4 is enabled in order to decode the serial address.

Then, the column predecoder 4 decodes the address signal SADDRi in order to supply a predecoded serial address signal PSAi to the column decoders 5_1-5_N after a time interval t_2 (refer to the timing chart of Figure 4D).

The column decoders 5_1-5_N generate signals for selecting an I/O gate after receipt of the serial address signal PSAi which is predecoded by the column predecoder 4.

If an I/O gate is gated by the output signals of the column decoders 5_1-5_N , then the data which has been transferred from the RAM port memory array 1 to the SAM port memory array 2 through a data transmission gate is outputted through the I/O

line.

Meanwhile, the tracking circuit 7 is for timing by use of an equivalent circuit path the time interval t_5 (i.e., $t_5=t_1+t_2+t_3+t_4$) which is required for the operations during the period when the data transferred to the SAM port memory array 2 is supplied through an I/O line to the I/O sense-amplifier 8. Specifically, this tracking circuit 7 is for: timing the time interval t_1 which is required for outputting a serial address SADDR_i by the serial counter 3 after receipt of a serial counting clock signal SC; timing the time interval t_2 which is required for outputting a predecoded serial address signal PSA_i after decoding the serial address SADDR_i by the column predecoder 4; timing the time interval t_3 (refer to the timing chart of Figure 4E) which is required for gating an I/O line after receipt of the predecoded serial address signal PSA_i by the column decoders 5₁-5_N; and modelling the time t_4 (refer to the timing chart of Figure 4F) which is required for supplying the data through the I/O line to the sense-amplifier 8 after the data is dispatched through the selected I/O gate from the SAM port memory array 2, in each case by use of an equivalent circuit path.

Thus, after the time intervals $t_5=t_1+t_2+t_3+t_4$ are tracked by the tracking circuit 7, if a tracking signal TRACK of Figure 4G is supplied to the I/O sense-amplifier 8 to activate it, then the I/O sense-amplifier 8 senses and amplifies the data supplied through the I/O line, and supplies a serial data to the data output buffer 9.

Meanwhile, the tracking signal is also supplied to

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the serial decoding disabling circuit 6, and therefore, after a data which is amplified by the I/O sense-amplifier 8 is

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supplied to the data output buffer 9 as shown in Figure 4H, the serial decoding disabling circuit 6 outputs a high state disabling signal SDD (Figure 4C) to the column predecoder 4 after a time interval t_6 . Therefore, as shown in Figure 4D, the column predecoder 4 is deactivated because of the serial address signal shifted to a high state, and the sensing operation as described above is no longer carried out.

That is, until the next falling edge of the serial counting clock is arrived, the operation of sensing the data of the SAM port memory array 2 is stopped.

After the termination of the data sensing operation as described above, if the rising edge of the clock signal SC arrives, the data which has been sensed by the above mentioned manner and stored in the data output buffer 9 before one and half cycles from the time t_1 in figure 4A is outputted through the I/O path 10. Of course, the data sensed shall be outputted after one and half cycles from the start of the time interval t_1 in Figure 4, and this can be illustrated as Figure 1B.

A detailed description about the data output with reference to a detailed circuit illustration will be provided afterwards.

Thus, it became possible to separate the data sensing time and the data outputting time in accessing to the data of the SAM port array.

Meanwhile, another method of decreasing the current according to an embodiment of the present invention will be described referring to Figure 4F.

When a data is supplied through the I/O line to the

I/O sense amplifier, if the I/O line is developed completely to the state of the power source voltage V_{cc} , then the developing time is extended, and the current flows through the register (not shown) of the SAM port during the extended time period.

However, in inhibiting the consumption current according to the present invention, the I/O line is open for a time period as long as the I/O sense-amplifier 8 can sufficiently develop the I/O line as shown in Figure 4F, and the rest of time is used in carrying out the precharging.

To describe it more specifically, in Figure 3, if the I/O line is precharged, then, in order to inhibit the DC current dissipation, the decoder circuits 4, 5₁-5_N for gating the I/O gate are disabled by means of the disabling clock generated from the serial decoding disabling circuit 6 described above. Therefore, the I/O line and the decoding circuits are operated during the period from the falling edge of the serial counting signal SC to the termination of the sensing. During the rest of the period, all the serial accessing circuits except the data output buffer 9 are disabled by the disabling circuit SDD.

Figure 5 illustrates in detail the circuit of the column predecoder 4 of Figure 3. In this figure, if a serial decoding disenabling signal SDD of a low state is supplied from the serial decoding disenabling circuit 6, then the column predecoding circuit 4 is enabled to decode the serial address signal SADDR_i supplied from the serial counter 3, and to output a column serial address signal PSA_i. On the other hand, if a

serial decoding disabling signal of a high state is supplied, then the column predecoder 4 is disabled, so that the operation of the column predecoder 4 should no longer be performed.

Figure 6 illustrates in detail the serial decoding disabling circuit 6, and this circuit 6 consists of: a section for delaying the serial counting clock signal SC until a serial address signal SADDRi is outputted after the serial counting clock signal SC is supplied; and a section for timing by use of an equivalent circuit path the time until a tracking signal TRACK is inputted from the tracking circuit after the outputting of a serial address ADDRi, and until the data sensing operation is completed.

The signal C3 is a control signal supplied from the external, and this signal is maintained at a low state during the serial data accessing operation.

Figure 7 illustrates in detail the tracking circuit, and the layout of this circuit is constituted in the same way as the layout of the signal path corresponding to the segment between the inputting of a serial counting clock signal SC and the supplying of the data to the I/O sense-amplifier 8 after the sensing of the data from the SAM port memory array 2.

Therefore, the tracking circuit 7 carries out the timing by use of an equivalent circuit path of the time until the sensed data is supplied to the I/O sense-amplifier 8 after the inputting of the serial counting clock signal SC thereto. Then the tracking circuit 7 outputs a tracking signal TRACK for controlling the I/O sense-amplifier 8 at the time when the data is supplied to the I/O

sense-amplifier 8.

As shown in Figure 4H, the I/O sense-amplifier 8 performs the amplifying operation only until the data sensed by the tracking signal TRACK of the tracking circuit 7 is supplied. After the completion of the amplifying operation of the I/O sense-amplifier 8, the serial decoding disabling circuit 6 outputs a serial decoding disabling signal SDD in accordance with the tracking signal, and thereupon, the column predecoding operation is stopped.

A signal C1 is for setting the serial accessing mode or the data transmission operating mode, and this signal is maintained at a high state when the data is serially accessed as is the case of the present invention. A signal C2 is a control signal supplied from the external, and this signal is maintained at a high state during the serial accessing to the data.

A signal C3 is disposed at the rear of the tracking circuit, and drives the transmission gate so as for a tracking signal to be outputted in relation with the serial data accessing operation, after the signal C3 is shifted to a low state during the serial accessing to the data of the dual port memory. On the other hand, during the data transmission mode, the signal C3 drives the transmission gate so that the transmission gate should output a tracking signal in relation with the data transmission operation.

Now their operation will be described in detail referring to Figures 8 and 4, Figure 8 being detailed circuit illustrations of the I/O sense amplifier 8 and the output

buffer 9 as described above, and Figure 4 being an illustration of timing charts for the circuits of Figure 8.

As shown by the detailed circuit illustration of Figure 5, the output signals PSA_i of the column predecoder 4 are supplied respectively to the column decoders 5_1-5_N , so that the corresponding column decoder should activate the I/O gate. Thus, the data are supplied from the SAM port memory array 2 to the I/O sense amplifier 8 (to be described below) in the form of I/O and I/O signals.

As shown in Figure 8, the I/O sense amplifier 8 and the corresponding output buffer 9 consist of a first latch and a second latch which are connected each other.

As mentioned in the beginning of this specification, the data outputting is carried out in such a manner that: at the falling edge of the SC clock, the data to be outputted is accessed and sense-amplified; and the data is stored into a two-stage buffer (to be outputted based on a pipeline method), i.e., into the first stage (the first latch) 81 among the first and second latches 81, 82. Thereafter, at the rising edge of the SC clock, there is outputted another data which has been sensed before one and half cycles, and has been stored in the second stage of the pipeline buffer, i.e., the second latch 82.

Then, at the falling edge of the SC clock, another data is sensed and amplified, and is supplied to the first latch 81, while the data which has been stored in the first latch 81 is transferred to the second latch 82. Thereafter, at the rising edge, the data which has been stored in the second latch 82 is outputted. This operation becomes apparent if

Figures 8 and 4 are referred to.

The first latch 81 includes a first transmitting gate 811, a first buffer 812 (consisting of two inverters), and a second transmitting gate 813, all of them being sequentially interconnected, while the second transmitting gate receives a signal ϕ_{PSOT} as a control signal from the outside.

Meanwhile, the second latch 82 includes: a second buffer 821 consisting of two inverters; and third and fourth transmitting gates 822, 823 to which the non-inverted output and inverted output of the buffer are respectively supplied. The third and fourth transmitting gates 822, 823 receive signals ϕ_{SOT} from the outside as the control signals.

Referring to Figure 4, at the falling edge of the SC clock, i.e., at the start of time interval t_1 , a high state signal ϕ_{PSOT} (Figure 4I) as a control signal is supplied to the first latch of the I/O sense amplifier.

Then, at the falling edge of the SC clock, a high signal is inputted as a control signal for the first transmitting gate 811 of the first latch 81 (the timing chart of Figure 4H), while the I/O sense amplifier 8 keeps the inputted data, i.e., the data sensed by the first latch 81. At the rising edge of the SC clock (at the time t_2 of Figure 4), the signals ϕ_{PSOT} ϕ_{SOT} and come low and high respectively, and therefore, the data which has been stored in the second latch, i.e., the data SDB' which has been existing since one and half cycles before the time t_2 , is outputted (SPOUT) through the buffer B in the form of a data SDB'' transformed from the data SDB', in accordance with the operations of the third and fourth

transmitting gates. The signal ϕ_{PSOT} is currently in a low state, and therefore, the data which is obtained at the sensing step is not transferred to the second latch 82, but is kept in the first latch 81.

Figure 4 illustrates the process of outputting the data to the output path 10 at the rising edge of the SC clock and at the time t_7 .

Then, at the time t_8 , a new data sensing is carried out, and in this state, the data existing at one and half cycles before the time t_7 has already been outputted. In this state, when the signal ϕ_{PSOT} is shifted to a high state, the data which is sensed at one and half cycles before the time t_8 is transferred to the second latch 82 in the form of SDB', while the data which is newly sensed is kept in the first latch 81 in the form of SDB.

Then, at the rising edge of the SC clock after one and half cycles from the start of the time interval t_1 , the data which is sensed after the start of the time interval t_1 is outputted.

According to the embodiments of the present invention described above, the time of sensing the data by accessing to the data of the SAM and the time of outputting the data to the outside are separated from each other, thereby reducing the peak current. Further, a tracking circuit for timing by use of an equivalent circuit path the data sensing operation is used in order to drive the I/O sense-amplifier and the column predecoder only during the required time, so that the consumption of the operating current should be kept to the minimum.



CLAIMS

1. A SAM data accessing method involving a low operating current in accessing the data which is supplied from a RAM port memory array through a transmission gate to a SAM port memory array to be stored therein, wherein at the falling edge of a serial counting clock signal, i.e., at one and half cycles before the outputting of the data, the data is sensed from said SAM memory array so as for the data to be stored in a first section of a pipeline type two-section buffer;

at the falling edge of the serial counting clock signal, i.e., at half cycles before the outputting of the data, the data stored in said first section of said two-section buffer is transferred to a second section of said two-section buffer to be stored therein; and

at the rising edge of the serial counting clock signal, the data stored in a second section of said two-section buffer is outputted.

2. A SAM data accessing method as claimed in claim 1, wherein the data sensing operation comprises: a stage of generating a serial address signal SADDRi in accordance with a serial counting clock SC; a stage of outputting a column predecoded address PSAi after decoding the serial address signal SADDRi; a stage of selecting the data from said SAM port memory array after decoding the column address PSAi and after gating an input/output gate; a stage of outputting a tracking signal by modelling the operations from the generation of the serial address to the amplification of the data selected from



said SAM port memory array; and a stage of amplifying the data sensed in accordance with the tracking signal.

3. A SAM data accessing method as claimed in claim 1 or 2, comprising a stage wherein, when the data sensed from said SAM is supplied through an input/output line to an input/output sense-amplifier, said input/output line is open only during a period as long as is sufficient for completely developing said input/output line by said input/output sense-amplifier; and during the rest of the time, a precharging is carried out, as well as disabling the decoding operation for gating said input/output line, thereby inhibiting the current consumption.

4. A SAM data accessing method substantially as herein described with reference to Figure 1B with or without reference to any of Figures 2 to 8 of the accompanying drawings.

5. A SAM data accessing circuit involving a low operating current, comprising: a serial counter for outputting a serial address by counting serial counting clock signals; column decoders for selecting an input/output gate; an input/output sense-amplifier for amplifying the data supplied through said input/output gate and an input/output line; a data outputting buffer for supplying to an input/output path the data amplified by said input/output sense-amplifier; a column predecoder for outputting a column decoder selecting signal after receipt of a serial address from said serial counter; a serial decoding disabling circuit for outputting an enabling



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signal to said column predecoder after receipt of a serial counting clock signal, and for outputting a disabling signal to said column predecoder after receipt of a tracking signal from a tracking circuit; and a tracking circuit for outputting a tracking signal after receipt of a serial counting clock signal in order to control said input/output sense-amplifier by forming a layout in the same form as that of the layout of the signal path between the inputting of a serial counting clock signal and the supplying of the data from a SAM port memory array to said input/output sense-amplifier; wherein a pipeline type two-section buffer is adapted to store in a first section data sensed from the input/output line one and a half periods before supplying data to the input/output path, to transmit the data from the first section to a second section half a period before supplying data to the input/output path, and to output the data from the second section at a rising edge of the serial counting clock signal.

6. A SAM data accessing circuit as claimed in claim 5, wherein said tracking circuit predecodes the output of said serial counter after receipt of a serial counting clock signal; said tracking circuit performs a timing by use of an equivalent circuit path of the time until the SAM data is supplied through an input/output line to said input/output sense-amplifier after said column decoders select an input/output gate upon receipt of the output signal of said column predecoder; and said tracking circuit also outputs a tracking signal to both said serial decoding disabling circuit and to said column predecoder



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when the sensed data is supplied to said input/output sense amplifier.

7. A SAM data accessing circuit substantially as herein described with reference to Figures 1B and 3 with or without reference to any of Figures 4 to 8 of the accompanying drawings.
