Claims

What is claimed:

1. A semiconductor device, comprising:

a semiconductor die;

an encapsulant deposited around the semiconductor die, wherein the encapsulant is disposed on a side surface of the semiconductor die;

a first insulating layer formed over a first surface of the semiconductor die;

a fan-in interconnect structure formed over the semiconductor die and first insulating layer, wherein the fan-in interconnect structure includes:

(a) a conductive layer formed over the semiconductor die and first insulating layer, and

(b) a second insulating layer formed over the conductive layer, and terminating within a footprint of the semiconductor die; and

a protection layer formed over a top surface of the encapsulant and coplanar with a second surface of the semiconductor die opposite the fan-in interconnect structure.

2. The semiconductor device of claim 1, wherein the conductive layer and second insulating layer are offset inwards from the side surface of the semiconductor die.

3. The semiconductor device of claim 1, wherein a thickness of the encapsulant disposed on the side surface of the semiconductor die is less than 100 micrometers.

4. The semiconductor device of claim 3, wherein the thickness of the encapsulant disposed on the side surface of the semiconductor die ranges from 30 to 50 micrometers.

5. The semiconductor device of claim 1, wherein a thickness of the encapsulant over the semiconductor die is at least 100 micrometers.

6. The semiconductor device of claim 1, further including a third insulating layer formed in direct contact with the first insulating layer, wherein the conductive layer is formed over the semiconductor die, first insulating layer, and third insulating layer.

7. The semiconductor device of claim 1, wherein the protective layer includes a transparent material or translucent material.

8. The semiconductor device of claim 6, wherein the conductive layer, the second insulating layer and the third insulating layer are offset inwards from the side surface of the semiconductor die.

9. A semiconductor device, comprising:

a semiconductor die;

an encapsulant deposited on a side surface of the semiconductor die;

a first insulating layer formed over a first surface of the semiconductor die;

an interconnect structure formed within a footprint of the semiconductor die and first insulating layer; and

a protection layer formed over a top surface of the encapsulant and over a second surface of the semiconductor die opposite the fan-in interconnect structure.

10. The semiconductor device of claim 9, wherein the interconnect structure includes:

a conductive layer formed over the semiconductor die and first insulating layer; and

a second insulating layer formed over the conductive layer.

11. The semiconductor device of claim 9, wherein a thickness of the encapsulant deposited on the side surface of the semiconductor die is less than 100 micrometers.

12. The semiconductor device of claim 11 wherein the thickness of the encapsulant deposited on the side surface of the semiconductor die ranges from 30 to 50 micrometers.

13. The semiconductor device of claim 9, wherein a thickness of the encapsulant over the semiconductor die is at least 100 micrometers.

14. The semiconductor device of claim 10, further including a third insulating layer formed in direct contact with the first insulating layer, wherein the conductive layer is formed over the semiconductor die, first insulating layer, and third insulating layer.

15. A semiconductor device, comprising:

a semiconductor die;

an encapsulant deposited around the semiconductor die, wherein the encapsulant is disposed on a side surface of the semiconductor die;

a fan-in interconnect structure formed over the semiconductor die; and

a protection layer formed over a surface of the encapsulant and over a surface of the semiconductor die opposite the fan-in interconnect structure.

16. The semiconductor device of claim 15, further including an insulating layer formed over a surface of the semiconductor die.

17. The semiconductor device of claim 15, wherein the fan-in interconnect structure includes:

a conductive layer formed over the semiconductor die; and

an insulating layer formed over the conductive layer.

18. The semiconductor device of claim 15, wherein a thickness of the encapsulant disposed on the side surface of the semiconductor die is less than 100 micrometers.

19. The semiconductor device of claim 15, wherein a thickness of the encapsulant over the semiconductor die is at least 100 micrometers.