Description

This invention relates to a semiconductor device having a metallisation structure for the interconnection of semiconductor components on a substrate and more particularly to a multilayered sputtered interconnect metallurgy structure which structure includes a low percent copper content aluminum/copper conductor.

Thin narrow interconnections have been used for some years for device interconnection purposes in the semiconductor integrated circuit industry. It is predicted that performance of these devices in the future will be limited by the performance of the device interconnection at the submicron level. At the submicron level, various technical problems are known to occur. While aluminum has been the preferred interconnection metal, as device dimensions are scaled down and current density increases, pure aluminum has been known to be susceptible to the problems of electromigration and hillock growth. To overcome the problems experienced with pure aluminum, aluminum has been alloyed with copper to form aluminum-copper. However, high percentage aluminum-copper (> 2%) is known to be difficult to dry etch and corrodes easily.

In an effort to improve on the use of aluminum-copper as the interconnection metallurgy, aluminum-copper has been taught to be layered with a refractory metal (i.e., U.S. Patent No. US-A-4,017,890). This patent teaches a method and resulting structure for forming narrow intermetallic stripes which carry high currents on bodies such as semiconductors, integrated circuits etc., wherein the conductive stripe includes aluminum or aluminum-copper with at least one transition metal. While the aluminum-copper and transition metal structure has been known to improve the electromigration problems associated with aluminum-copper, the problems of etching and corrosion, as well as, the complete elimination of hillocks have not been solved.

As known in the art, hillocks are known to result from the large differences between the thermal expansion coefficients of the metal interconnect lines and the substrate. To eliminate and minimize hillock formation, it has been known in the art to use a multilayered structure instead of a single layer of the interconnect metallurgy. An effective reduction in hillock formation has been found to be achieved by using a multilayered structure of aluminum or aluminum intermetallic with a layer of refractory metal. Wherefore, a typical interconnect metallurgy structure would comprise a layered structure of aluminum silicon compound onto which there has been deposited, a layer of refractory metal, such as, titanium (see article "Homogeneous and Layered Films of Aluminum/Silicon with Titanium For Multilevel Interconnects", 1988 IEEE, V-MIC Conference, June 25-26, 1985).

There have also been refinements to this layered metal structure to provide a lower resistivity, hillock free, interconnect metallurgy. These refinements include the incorporation of a barrier metal of, for example, titanium tungsten or titanium nitride under the aluminum silicon to prevent contact spiking and prevent the formation of ternary compounds in the aluminum silicon alloy (see article "Multilayerd Interconnections For VLSI" MRS Symposia Proceedings, Fall, 1987).

In addition, in this area, there have also been other proposed device interconnect structures to reduce resistivity and provide a more planar and defect free interconnect structure.

For example, IBM Technical Disclosure Bulletin, Vol. 21, No. 11, April, 1979, pp. 4527-4528, teaches the enhancement of the metallurgy for the interconnection due to sputtered deposition. Moreover, the feature of using a capping layer to improve performance has been proposed in IBM TDB Vol. 17, No. 1A, 1984 and TDB Vol. 21, No. 2, July 1978. However, no structure has been discovered which can satisfy all performance criteria providing a low resistance, hillock free, corrosion resistant, etchable, interconnection metallurgy structure.

It is, therefore, an object of the present invention to provide sputtered low weight percent copper (< 2%) content aluminum/copper conductor for device interconnection on a substrate with superior electromigration characteristics.

It is a still further object of the present invention to develop a multilayered interconnect metallurgy structure that is hillock free, dry etchable and corrosion resistant.

It is another object of the present invention to provide a multilayered interconnect metallurgy structure which has a low resistivity.

A semiconductor device having a sputtered low-copper concentration multilayered, component interconnect metallurgy structure is set out in Claim 1, a method of forming such a device is set out in Claim 5. The interconnect metallization structure comprises a sputtered aluminum-copper (<2%) weight percent copper conductor. In the preferred embodiment, the conductor layer is formed with a top and bottom layer of an intermetallic, said intermetallic also being sputtered and being of a thickness of approximately 70nm. Onto said intermetallic layer is further deposited an etch stop, and non-corrosive, protective capping layer.

FIG. 1 is a cross-sectional view of the preferred embodiment of an interconnect metallurgy according to the subject invention.

FIGS. 2 through 8 are cross-sectional views of the process for building the preferred interconnect metallurgy of the subject invention in a step-by-step fashion.

FIG. 9 is a graph of the lifetime (hours) versus weight percent copper for interconnect metallurles of the

subject invention as compared to prior art interconnect metallizations.

FIG. 10 is a graph of the resistivity versus weight percent copper for various alternative embodiment metallurgies of the subject invention before and after anneal.

FIG. 1 is a cross-sectional view of the preferred embodiment of an interconnect metallurgy structure according to the subject invention. FIG. 1 represents the interconnect structure after being processed through final annealing.

Referring to FIG. 1, the interconnect metallurgy is seen to comprise a four-layer structure over an interplanar stud connection (10) surrounded by an insulator 8 to make connection to a device substrate 6. The four-layer structure consists of an intermetallic bottom layer 12' typically 70nm thick and, in a preferred embodiment would comprise $TiAl_3$.

Above is a low percent (< 2%) weight percent copper, aluminum-copper, conductor layer 14. At the end of the process, layer 14 is typically 850nm thick and consists of a composition of 99,5% aluminum and 0,5% copper (aluminum-0,5% copper hereafter). On layer 14 is a second intermetallic layer 16' of the same thickness and composition as layer 12'. Finally, a layer 18 of aluminum-0,5% copper (or pure aluminum) of approximately 10nm to 50nm thick achieves the structure. While this completes the structure for a single interconnect layer according to the subject invention, it should be recognized by those skilled in the art that said layers can then be repeated in a multiple level sequence to complete the interconnect circuit for the devices.

Referring now to FIG. 2, FIG. 2 shows a planar insulator 8 and contact stud 10 with a Group IVA metal layer 12 sputter deposited thereon. The layer 12 is deposited by the following process. After formation of the device contact metallization 10, the semiconductor wafer would be loaded into a sputtering tool which has been pumped to a low pressure. An in- situ sputter clean is then performed to remove any oxide from the contact metal 10 formation on the wafer at this time. This in-situ sputter clean typically is a mild sputter clean, run, for example, at about five minutes at low power (approximately 1000 watt) in a high-pressure argon ambient.

Following the sputter cleaning, the first level of metallization 12 is then deposited. This first level metallization 12 is comprised of a Group IVA metal, preferably titanium, deposited on the device contact metallization 10 of the wafer in a blanket formation. This layer 12 is deposited at low power in a high pressure, high purity, argon plasma from an ultra-pure titanium target at a rate of about 6nm per minute. Preferably, the titanium is deposited to a thickness of approximately 25nm. Referring now to FIG. 3, following the deposition of the layer 12, the interconnect metallization layer 14 is next blanket deposited. The interconnect metallization 14 is preferably aluminum-0,5% copper (approximately 950nm thick). The aluminum-copper is deposited at high power using a direct current magnetron in a high purity argon plasma from an ultra-pure pre-alloyed target typically aluminum-0.5 weight percent copper with a deposition rate of about 150nm per minute.

Onto said aluminum-copper interconnect metallization 14 is then deposited 25nm of a Group IVA metal similar to the previously deposited metal layer 12 discussed above. Deposition, composition and thickness of said layer 16 is identical to the previously deposited layer 12 (FIG. 4).

From FIG. 5, onto said metal layer 16 is then blanket deposited a suitable capping layer 18 to complete the interconnect metallurgy at this level. The capping layer 18 is preferably comprised of aluminum-0.05% copper deposited in the same manner as the conductor aluminum-0.5% copper layer 14 as discussed above. The purpose of this layer is to: 1) prevent over-etch of metal layer 16; 2) limit the amount of light reflection during the subsequent photoresist steps, and 3) to act as a protective layer against corrosion during subsequent processing. Therefore, any layer which would similarly satisfy the requirements of reducing the amount of light reflection and provide protective anodic capping during subsequent processing would be usable for this layer (e.g. pure aluminum).

Referring now to FIG. 6, on top of metallization 18, a multilayered photoresist (20, 22 and 24) is then applied to pattern this blanket interconnect metallization. Any number of different photoresist techniques can be used. In particular, multilayered photoresists are well suited for this purpose, as well as, single-layered resists.

With a multilayered resist as shown in FIG. 6, a first resist 20 is applied to a thickness of approximately 1.8 µm. In the preferred embodiment this resist is a diazo-quinone novolak photoresist. The resist 20 is baked in an oven in a nitrogen ambient at about 200°C for 30 minutes. This resist 20 serves as a sacrificial layer during subsequent metal reactive ion etching (RIE).

Onto said resist 20 is then deposited 20nm of a silylating agent 22, such as, HMDS (hexamethyldisilizane). The HMDS 22 serves as a barrier to the oxygen reactive ion etching which is used to pattern the imaging layer resist 24.

Onto said HMDS layer 22 is next deposited an imaging layer resist 24 to a thickness of about 0.9-1.2 micrometers. Similar to resist 20, imaging resist 24 is a diazo-quinone novolak positive photoresist. The HMDS 22 and imaging resist layer 24 are then baked on a hot plate for 25 minutes at 85°C.

The imaging layer resist 24 is then exposed for the specific time required when used in conjunction with a specific exposure tool and associated mask. The exposed image is developed using conventional developing for

the required time depending on the exposure. The wafer is then rinsed and dried and the patterned top imaging layer is UV hardened by exposing it to ultraviolet light for a specific period of time, typically, 5 to 10 minutes.

Following the patterning of the top imaging resist 24, the HMDS 22 and resist layer 20 are ready to be removed to expose the metal. The HMDS 22 and the resist 20 are removed by reactive ion etching. This is accomplished by loading the wafer into a plasma tool and exposing the wafer to a plasma reactive to the HMDS layer 22 (e.g. CF_4) and then to a different plasma (e.g. O_2) reactive to resist 20. The polymer residues of the remains of the HMDS layer 22 and the resist 20 are then removed by dipping in a solution of a conventional cleaning etch solution. This reactive ion etching of the HMDS layer 22 and the resist 20, has put a lithographic mask into place for the subsequent reactive ion etching of the underlying blanket metal layers.

The metallurgy can now be reactively ion etched in a multi-step sequence. The first step is to break through any oxides which may exist on the top surface of the metallization. Next, most of the metal is removed by reactive ion etching. An over etch is, then, performed to insure that all of the metal in the previous step has been etched away. Finally, a passivation step is performed to prevent any metal corrosion.

The reactive ion etch is typically performed in a single wafer tool under a low pressure. Typical plasma composition, pressure, power and time combinations, for performing the above etches in a step-by-step process can be seen from the following Table I. These compositions, pressures, powers and times should be recognized by those skilled in the art as being designed for a specific tool under specific conditions Any comparable times, compositions, pressure, etc., could be similarly fabricated to insure the etch of the blanket metallization.

Table I

	Gas Flow (cc/min)			
	Step 1	Step 2	Step 3	Exit
BCl_3	20	12	12	---
Cl_2	11	11	8	---
$CHCl_3$	5	16	16	---
N_2	50	50	50	---
CF_4	---	---	---	180
O_2	---	---	---	20
Pressure (Pa)	50	50	50	60
Power (Watts)	485	350	350	130
Typical Times	15 sec	2-3 min	40 sec	20 sec

With the completion of the reactive ion etch, the wafer can then be rinsed and dried.

Referring now to FIG. 7, it can be seen that the reactive ion etch of the metal removes any of the remaining imaging layer resist 24 and most of the the HMDS layer 22 leaving on the surface of the metal the resist 20. This resist 20 can be removed by placing the wafer in an oxygen plasma for approximately 45 minutes. The wafer is then placed in a developer at room temperature for a short period of time to remove any oxides that may have formed in the previous step. The wafer is again rinsed and dried.

With removal of this final layer of the resist 20, the metallization stack can now be annealed by placing the wafer in an oven at 400°C in forming gas for 1 hour in order to form $TiAl_3$ intermetallic layers 12' and 16' on the top and the bottom of the aluminum-copper layer 14 and to allow grain growth to occur in the aluminum-copper layer 14.

From FIG. 8, it can be seen that once the metallization stack has been annealed (to the structure of FIG. 1) a suitable insulator 26 (e.g., planar quartz or plasma-enhanced CVD oxide or an organic insulator such as polyimide) can be blanket deposited over the multilayered interconnect structure. This insulator 26 can then be planarized and/or patterned for stud connection to the repeating interconnect layers deposited onto the base interconnect layer.

The superior performance of the interconnect metallurgy of the subject invention over that which is known

in the prior art can be seen in the following figures. FIG. 9 is a lifetime (hours) versus weight percent copper graph for the electromigration characteristics of both the above-described sputtered four-layered structure and an alternative sputtered three-layer structure (Al/Cu/refractory metal/Al-Cu), as compared to an evaporated three-layer structure patterned by lift-off and an evaporated four-layer structure, patterned by RIE. From FIG. 9 it can be seen that for all weight percent copper compositions, the sputtered interconnect metallurgies are vastly superior to the evaporated metallurgies.

Fig. 10 is a graph of the resistivity versus weight percent copper for various alternative embodiment metallurgies of the subject invention. The metallurgies have been subjected to a 400°C forming gas anneal wherein the plots have been taken both before and after said anneal. From the plots it can clearly be seen that the resistivity of the 0.5 weight percent copper structures are lower than that of the higher weight percent copper films. Additionally, it can also be seen that the annealed films of the four-layer structure have a lower resistivity than the annealed films of the three-layer structure.

The following Table II is a further comparison of the electromigration characteristics of sputtered Al-0.5%Cu metallurgy after annealing with intermetallic formation as compared to various other interconnect metallurgies.

TABLE II

ALLOY	RESISTIVITY ($\mu\Omega$ - cm) 1hr, 400°C Forming Gas	T(50%) 250°C, 2.5×10^6 A/cm^2 (Hours)
Al-0.5%Cu (Ref.#1)	3.5	9000
Al-0.5%Cu (Ref.#2)	3.4	12000
Evap (Ref. #3)	3.7	400-500
Evap (Ref. #4)	3.8	400-500
Cr/Al-4%Cu	3.0	400
Al	2.8	15
Al-0.5%Cu	2.9	50
Al-1.2%Si-0.15%Ti	3.1	23
Al-1.2%Si (Ref.#5)	2.9	156*
Al-1%Ti	6.6	2
Al-Si/Ti (Ref.#6)	3.1	300*

* 150°C, 10^6 A/cm^2, unpassivated

1. Sputtered 425nm Al-0.5%Cu/150nm $TiAl_3$/425nm Al-0.5%Cu and annealed in forming gas at 400°C.

2. Sputtered 70nm $TiAl_3$/850nm Al-0.5%Cu/70nm $TiAl_3$/25nm Al-0.5%Cu and annealed in forming gas at 400°C.

3. Evaporated 425nm Al-0.5%Cu/150nm $TiAl_3$/425nm Al-0.5%Cu and annealed in forming gas at 400°C.

4. Evaporated 70nm $TiAl_3$/850nm Al-0.5%Cu/70nm

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5. F. Fisher, Siemens Forsch-U. Entwickl-Dec. 13, 21 (1984).

6. D.S. Gardner, T.L. Michalka, P.A. Flinn, T.W. Barbee Jr., K.C. Saraswat & J.D. Meindl, Proc. 2nd IEEE VMIC, pp. 102-113 (1985).

From the table it can be seen that the sputtered 0,5% copper metallurgy provides the longest electromigration capability with the lowest resistivity.

In general, while the corrosion resistance of bulk aluminum is greatly decreased by the addition of copper, it is known and recognized in the art: (see, for example, J. Zahavi, M. Rotel, H.C.W. Huang, P.A. Totta, "Corrosion behavior of Al-Cu Alloy Thin Films in Microelectronics." Proceedings of International Congress of Metallic Corrosion. Toronto, June, 1984.) that the corrosion resistance of reactive ion etched low copper containing films of aluminum (e.g., less than 1% copper) are at least as good as bulk aluminum. This is in contradiction to that skill in the art which recognizes that the corrosion resistance of higher percentage (above 1%) copper-aluminum films significantly degrades below that of pure aluminum. While detailed understanding of the mechanism of the performance of the subject interconnect metallurgy is not known, several principles have been extended by the inventors to explain the superior electromigration and resistivity results as seen above.

The solubility of copper and aluminum is known to decrease from 5,65 wt.% at 548°C to 0,25 wt.% at room temperature. Therefore, the 0.5% copper film composition of the subject invention has enough copper without theta phase formation to improve both the mechanical properties and reliability, (e.g., electromigration properties) of the alloy over pure aluminum. Moreover, it is recognized that there is enhanced copper uniformity in the subject films due to the fact that said films were sputtered versus the non-uniformity in copper distribution as can be seen in the evaporated aluminum-copper films. In addition, it is also recognized that evaporation results in the uneven distribution of theta particles in the evaporated films which uneven distribution is known to contribute to the poor mechanical corrosion and electrical properties of the prior art films. The superior mechanical and electrical properties of the subject metallurgy is therefore directly attributed to the enhanced copper uniformity in these films as result of the deposition by sputtering. Therefore, an improved sputtered copper interconnect metallurgy has been developed that has enhanced reliability, lower resistivity, is dry etchable, and has a superior corrosion resistance than that metallurgy as presently used in the prior art. The preferred sputtered (4-layer) metallurgy exhibits lower resistivity and superior electromigration over a wider range of copper compositions than previous prior art structures.

Claims

1. A semiconductor device including a substrate and a metallization structure for the interconnection of semiconductor components on said substrate said metallization structure comprising:
   a) a layer (14) of sputter deposited aluminum-copper of greater than 0% and less than 2% copper by weight; and
   b) an intermetallic layer (16) formed at the surface of said aluminum-copper layer, said intermetallic layer formed of a sputter-deposited metal selected from the group including titanium, zirconium and hafnium, and aluminum of said aluminum-copper layer.

2. The semiconductor device of Claim 1 further comprising:
   c) an intermetallic layer (12) formed between said substrate and said layer a) (14) of sputter deposited aluminum-copper, said intermetallic layer formed of a sputter-deposited metal selected from the group including titanium, zirconium and hafnium, and aluminum of said aluminum-copper layer.

3. The semiconductor device of claim 2 further comprising:

$TiAl_3$/25nm Al-0.5%Cu and annealed in forming gas at 400°C.

5. F. Fisher, Siemens Forsch-U. Entwickl-Dec. 13, 21 (1984).

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Claims

1. A semiconductor device including a substrate and a metallization structure for the interconnection of semiconductor components on said substrate said metallization structure comprising:
   a) a layer (14) of sputter deposited aluminum-copper of greater than 0% and less than 2% copper by weight; and
   b) an intermetallic layer (16) formed at the surface of said aluminum-copper layer, said intermetallic layer formed of a sputter-deposited metal selected from the group including titanium, zirconium and hafnium, and aluminum of said aluminum-copper layer.

2. The semiconductor device of Claim 1 further comprising:
   c) an intermetallic layer (12) formed between said substrate and said layer a) (14) of sputter deposited aluminum-copper, said intermetallic layer formed of a sputter-deposited metal selected from the group including titanium, zirconium and hafnium, and aluminum of said aluminum-copper layer.

3. The semiconductor device of claim 2 further comprising:

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d) a metal overlayer (18) deposited on layer (b) (16).

4. The semiconductor device of Claim 3 wherein said metal overlayer d) (18) is aluminum-copper alloy containing greater than 0% to less than 2% copper by weight.

5. A method of forming a semiconductor device including a substrate and a metallization structure for connecting semiconductor components on said substrate, said method comprising the steps of:
a) sputter depositing a first layer (12) of at least one of the metals selected from the group including titanium, zirconium and hafnium onto said substrate,
b) sputter depositing onto said first layer a second layer (14) of aluminum copper of greater than 0% and less than 2% copper by weight,
c) sputter depositing a third layer (16) of the same metal as in step a, and
d) annealing the structure to form an intermetallic of the selected metal and aluminum.

Patentansprüche

1. Halbleiterbauelement mit einem Substrat und einer Metallisierungsstruktur für die Verbindung von Halbleiterkomponenten auf dem Substrat, wobei die Metallisierungsstruktur folgendes beinhaltet:
a) eine Schicht (14) aus durch ein Sputterverfahren aufgebrachtem Aluminium-Kupfer mit mehr als 0 Gew.-% und weniger als 2 Gew.-% Kupfer; und
b) eine Schicht (16) aus einer intermetallischen Verbindung, die auf der Oberfläche der Schicht aus Aluminium-Kupfer ausgebildet ist, wobei die Schicht aus der intermetallischen Verbindung aus einem durch ein Sputterverfahren aufgebrachten Metall, das aus der Gruppe ausgewählt ist, die Titan, Zirkonium und Hafnium beinhaltet, und Aluminium der Aluminium-Kupfer-Schicht gebildet wird.

2. Halbleiterbauelement nach Anspruch 1, des weiteren enthaltend:
c) eine Schicht (12) aus einer intermetallischen Verbindung, die zwischen dem Substrat und der Schicht a) (14) aus durch ein Sputterverfahren aufgebrachtem Aluminium-Kupfer gebildet wird, wobei die Schicht aus der intermetallischen Verbindung aus einem durch ein Sputterverfahren aufgebrachten Metall, das aus der Gruppe ausgewählt ist, die Titan, Zirkonium und Hafnium beinhaltet, und Aluminium der Aluminium-Kupfer-Schicht gebildet wird.

3. Halbleiterbauelement nach Anspruch 2, des weiteren enthaltend:
d) eine Deckschicht (18) aus Metall, die auf der Schicht b) (16) aufgebracht ist.

4. Halbleiterbauelement nach Anspruch 3, wobei die Deckschicht d) (18) aus Metall aus einer Aluminium-Kupfer-Legierung besteht, die mehr als 0 Gew.-% und weniger als 2 Gew.-% Kupfer enthält.

5. Verfahren zur Herstellung eines Halbleiterbauelementes mit einem Substrat und einer Metallisierungsstruktur zum Verbinden von Halbleiterkomponenten auf dem Substrat, wobei das Verfahren die folgenden Schritte beinhaltet:
a) Aufbringen einer ersten Schicht (12) aus wenigstens einem der Metalle, die aus der Gruppe ausgewählt werden, die Titan, Zirkonium und Hafnium beinhaltet, durch ein Sputterverfahren auf das Substrat,
b) Aufbringen einer zweiten Schicht (14) aus Aluminium-Kupfer mit mehr als 0 Gew.-% und weniger als 2 Gew.-% Kupfer durch ein Sputterverfahren auf die erste Schicht,
c) Aufbringen einer dritten Schicht (16) aus dem gleichen Metall wie in Schritt a) durch ein Sputterverfahren und
d) Tempern der Struktur, um eine intermetallische Verbindung aus dem ausgewählten Metall und Aluminium zu bilden.

Revendications

1. Dispositif semi-conducteur comprenant un substrat et une structure de métallisation pour l'interconnexion de composants semi-conducteurs sur ledit substrat, ladite structure de métallisation comprenant :
a) une couche (14) d'aluminium-cuivre déposée par vaporisation, à plus de 0% et moins de 2% de cuivre en poids ; et

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b) une couche intermétallique (16) formée sur la surface de ladite couche d'aluminium-cuivre, ladite couche intermétallique étant formée d'un métal déposé par vaporisation choisi dans le groupe comprenant le titane, le zirconium et le hafnium, et l'aluminium de ladite couche d'aluminium-cuivre.

2. Dispositif semi-conducteur selon la revendication 1, comprenant en outre :
c) une couche intermétallique (12) formée entre ledit substrat et ladite couche a) (14) d'aluminium-cuivre déposée par vaporisation, ladite couche intermétallique étant formée d'un métal déposé par vaporisation choisi dans le groupe comprenant le titane, le zirconium et le hafnium, et l'aluminium de ladite couche d'aluminium-cuivre.

3. Dispositif semi-conducteur selon la revendication 2, comprenant en outre :
d) une surcouche (18) métallique déposée sur la couche b) (16).

4. Dispositif semi-conducteur selon la revendication 3, dans lequel ladite surcouche métallique d) (18) est un alliage d'aluminium-cuivre contenant plus de 0% et moins de 2% de cuivre en poids.

5. Procédé pour former un dispositif semi-conducteur comprenant un substrat et une structure métallique pour connecter des composants semi-conducteurs sur ledit substrat, ledit procédé comprenant les étapes consistant à :
a) déposer par vaporisation une première couche (12) d'au moins un des métaux choisis dans le groupe comprenant le titane, le zirconium et le hafnium sur ledit substrat,
b) déposer par vaporisation sur ladite première couche une seconde couche (14) d'aluminium-cuivre comprenant plus de 0% et moins de 2% de cuivre en poids,
c) déposer par vaporisation une troisième couche (16) du même métal que dans la couche a),
d) recuire la structure pour former un intermétallique du métal choisi et de l'aluminium.