Description

This invention relates to electronic component packaging and particularly to semiconductor device packages as set out in the preamble to the main claim.

Such a package is known from U.S. patent 4,038,488 in which two chips are mounted in cavities arranged in tandem. Further reduction of overall package dimensions and increase of the degree of integration and density of packaged devices is still required, however.

A device package is known from U.S. patent 4,167,647 in which two semiconductor chips are mounted in respective cavities which are disposed back-to-back on a common substrate. The only interconnections which are provided in this package are with external terminal leads.

In the device package as claimed, not only are the cavities disposed back-to-back but conductors providing interconnections are disposed between the cavities.

An embodiment of the invention will now be described by way of example with reference to the accompanying drawings in which:

FIG. 1 is a package according to the invention with its cover removed, partially cut away and in perspective, and

FIG. 2 is an exploded view of the package of FIG. 1.

The perspective view of FIG. 1 shows a double-cavity semiconductor chip carrier 100 partially cut away to show a semiconductor chip 101 mounted in the upper cavity of the carrier. The second cavity similarly opens from the opposite or under-surface 109 of the carrier so that a second semiconductor chip is mounted in back-to-back relation with ceramic layer between the chips. Although not shown, a cover member is sealed to the metallized area 107 to enclose the upper chip cavity and similar means are used to enclose the lower cavity by sealing to the metallized area indicated by the dotted outline 82 on ceramic chip 80 of FIG. 2.

The semiconductor chip 101 is mounted to a metallized area 105 in the bottom of cavity 108 and wire leads 104 connect from contact pads on the semiconductor chip to the internal terminal portions of metallization patterns 106 on the carrier. Vertical interconnection within the carrier is effected by the metallized grooves or castellations 103 and by conductive paths 110 which will be hereafter termined vias 110. These interconnection means and combinations of such means will be disclosed in more detail hereinafter in connection with the description of FIG. 2.

FIG. 2 is an exploded perspective view of the series of ceramic members which, when assembled, constitute the double cavity semiconductor chip carrier device. Each of the ceramic members 10, 20, 40, 50, 60, 80, 90 is a green or uncured ceramic member essentially of alumina (Al_2O_3). Typically, one suitable ceramic used for this purpose is 7231A green ceramic sheet marketed by Plessey Frenchtown, Frenchtown, New Jersey. This ceramic material is furnished in sheets which are shaped by pressing, molding, and punching to conform to the configurations of the various members shown in FIG. 2.

In addition to the shaping operations as required, the ceramic members 10, 20, 40, etc., are provided with metallization patterns to produce the desired electrical interconnections within the carrier as well as the internal and external terminals for making connection to the electrodes on semiconductor chips and for interconnecting the carrier to external circuitry. Typically these metallization areas are produced by deposition using masking or screening techniques to apply successive layers of suitable metals. In this specific embodiment, the metallized areas comprise a composite layer of tungsten applied directly to the ceramic, covered with a layer of nickel and finally a layer of gold. Vertical interconnection also is provided by internal vias comprising vertical holes which are filled with metallic paste which is converted to a solid electrically conductive form.

The two chip-receiving cavities of the double cavity carrier are defined each by the combination of annular ceramic members and a solid mounting member. Thus, one cavity is formed by ceramic members 10 and 20 having respective central openings 11 and 21 mounted on ceramic member 40 which has the mounting means at the bottom of the cavity comprising the mounting pad 41. Similarly, the downward facing cavity is formed by ceramic members 80 and 60 having respective openings 81 and 61 and mounting member 50 including the mounting pad defined by broken line 51.

Semiconductor chips 25 and 64 are shown with wire leads 27, 67 interconnecting chip contact pads 26, 66 and internal terminals 28, 68 at the level at which they are positioned in the completed carrier. Typically, these wire leads are attached by wire bonding techniques such as thermocompression bonding or ultrasonic bonding. Each semiconductor chip further is mounted and connected to its appropriate mounting pad. It will be understood that mounting and interconnection of the semiconductor chips is done in the assembled carrier.

In this specific embodiment, the peripheral edges of the ceramic members contain a series of notches or grooves, such as the grooves 14 of the member 10. These grooves, termed castellations, are metallized to provide conductive paths on the outer edges of the assembled carrier. Vertical interconnection within the carrier also is provided by means of internal vias 55 shown in connection with member 50. The vias are made by filling selectively formed holes in the ceramic members with a metallic paste which during the ceramic firing process results in the pipe-like electrically conductive vias. The extent and location of vias is determined by the location and alignment of holes 23 in member 20 and holes 43 in member 40, for example.

Horizontal interconnection within the carrier is

provided primarily by the metallized leads 22 on member 20, leads 53 on member 50, for example, which largely are embedded in the completed carrier.

Thus, to recapitulate, for the specific embodiment of FIG. 2, annular ceramic member 10 defines, in part, the upper cavity and includes a metallized area 12 on the top surface to which a coverplate is sealed. The metallized area 12 is shown connected to edge castellation 13 for electrical grounding and shielding purposes where desirable.

Ceramic member 20 corresponds to the level at which the upper semiconductor chip 25 is mounted and includes on its upper surface an array of metallized leads 22. The innermost ends of these metallized leads 22 constitute internal terminals 28 disposed around the periphery of the cavity containing the semiconductor chip 25. As previously noted, interconnection between contact pads 26 on the semiconductor chip and the terminals 28 are made by means of wire leads 27 which typically are wire bonded to both contacts. Certain of the metallized leads 22 connect to the peripheral castellations 29, for example. Other of the metallized leads 24, for example, encompass a via hole 23. Thus, the horizontal metallized leads may connect either to the peripheral metallized castellations or to vias or both, for vertical interconnection. These arrangements provide great flexibility in formulating interconnection patterns.

Largely for reasons relating to ease of fabrication the underside of member 20 does not contain metallized leads except for emerging vias. Generally, in this specific embodiment the ceramic members have metallized leads on only one face of the members except for the central layer member 50, described specifically hereinafter.

Ceramic member 40 is a solid, rather than annular member and the metallized area 41 is the so-called mounting area for the semiconductor chip 25 and thus is the bottom of the upward facing chip cavity. Shown also are via holes 43 and peripheral castellations 42, to one of which the metallized area 41 is connected by means of metallized lead 44.

Ceramic member 50, as noted above, is the central layer of the carrier and has on its upper surface metallized leads 53 and vias 55 occupying via holes 54. It will be understood that although the vias 55 are shown with rod-like appearance, they do not exist separately in this form. They are shown in this fashion to indicate their electrically conductive function. The metallized leads 53 on ceramic member 50 are shown interconnecting vias 55 and peripheral conductive castellations 52. They may also interconnect vias or peripheral castellations or both. On the underface of member 50 dotted outline 51 indicates the chip-mounting area for semiconductor chip 64 which is mounted in the lower facing cavity of the carrier. As in the case of chip-mounting area 41, area 51 likewise is connected to a vertical interconnect which may be to the same pheripheral castellation 52 or to a different connection.

Annular ceramic member 60 defines, in part, the lower chip cavity and is similar in structure and function to ceramic member 20. However, the metallized leads 62 on the underface of member 60 are not necessarily the same as those provided on the upper face of ceramic member 20.

In this specific embodiment, ceramic member 80 is somewhat analogous to ceramic member 10 in that dotted outline 82 represents a metallized area on the underface of the member to which the lower cover member, not shown, may be attached, typically by a metal-to-metal hermetic seal in the same manner as the top cover.

However, in this embodiment there is an additional annular ceramic member 90 below member 80 which has the primary function of carrying the external terminals 93 shown in dotted outline as metallized areas on the underface of member 90. These terminals 93, arranged around the periphery of the member sometimes referred to in the art as the contact footprint of the carrier. As external terminals they enable contact to corresponding contact arrays in apparatus boards of various types. In one embodiment, the external terminals 93 contact solder bumps on the face of a mounting board which ensure clearance between the underside of the carrier and the surface of the apparatus board.

Connection from the conductive circuits of the upper portion of the carrier to the external terminals 93 is made from the peripheral castellations 83 of member 80 to short metallized leads 84 on the underface of member 80. Vertical connection through member 90 then is made by means of short vias 92 which contact the external terminals 93. In this specific embodiment, member 90 has no peripheral castellations and the non-indented periphery of this member acts as a solder stop to prevent solder flow up the castellations when the lower contact face of the carrier is solder dipped. It is possible, of course, in the alternative to provide peripheral conductive castellations on member 90, particularly if a solder stop is not necessary.

Alternative embodiments also are possible in which either the vias or the peripheral castellations are omitted entirely from the carrier. For such arrangements, either conductive vias or peripheral castellations alone are relied upon for vertical interconnection.

As can be seen from the relative dimensions, the cover member for the lower cavity of the carrier fits within the opening 91 of member 90 and thus, does not protrude below the under or contact face of member 90. In this connection, it will be understood that hermetically sealed cavities may not always be required and a cover member may be omitted or be of the non-hermetic type for mechanical protection only.

When the series of ceramic members 10, etc., are sandwiched together and the via holes filled with the metallic paste, the assembly is fired to produce a unitary member comprising the double cavity semiconductor chip carrier. In the unitary assembly interconnections may be made from particular contact pads on each of the mounted semiconductor chips through the various metallization leads to terminate in certain of the external terminals 93 on the bottom face of the carrier. Interconnection between particular contact pads on the semiconductor chips also can be made. It will be evident that, in the typical instance, in which both semiconductor chips are of the integrated circuit type a considerable flexibility of interconnection is possible, even for a given design of carrier. In particular, computer programming can be used to determine the interconnection pattern for particular semiconductor devices which are paired in particular double cavity carriers of this general configuration. Within the general carrier configuration, as previously noted, various designs may be fabricated to have different interconnection arrangements. These different arrangements may be obtained by relatively simple variations in metallization masks and via patterns.

The perspective view of FIG. 1 illustrates the carrier in its assembled form showing the upper cavity with a semiconductor chip installed therein. It will be apparent that the overall length-width dimensions of the carrier are similar to those for a single chip carrier while the double cavity carrier requires only slightly greater thickness than that used for a single chip carrier. Thus the double cavity chip carrier can be fitted into recesses which are not substantially greater than those previously required for single chip carriers, thereby greatly increasing the device density attained in particular circuit apparatus. As set forth above the feature relating to interconnection flexibility with the double cavity chip carrier greatly increases the degree of integration attainable without changes in device designs and standards.

Moreover, although the double cavity carrier is described as a semiconductor chip carrier, and particularly in terms of an integrated circuit chip, it will be appreciated that other similar electronic elements may be included. For example, the mounted elements may include discrete semiconductor devices, capacitors, resistors, and piezoelectric devices. In particular, a double-cavity carrier may include an integrated circuit chip and a crystal unit, or an MOS capacitor and a hybrid integrated circuit.

Claims

1. A semiconductor device package comprising a chip carrier (100) including a pair of cavities (21, 61) each having a semiconductor chip (25, 64) mounted therein, the chip carrier being made from a plurality of layers (10—90) of insulative material, horizontal first conductors (24, 53) on a horizontal surface of each of a plurality of said layers, second conductors (27, 67) interconnecting the semiconductor chips to certain of the first conductors, a plurality of vertical third conductors (55) each extending through a plurality of said layers to interconnect first conductors of different layers, and external terminals (93) mounted peripherally on one of said layers to permit selective electrical contact to the second conductors by way of the first conductors and third conductors, characterized in that the cavities (21, 61) are disposed in back-to-back relationship with the carrier, the backs of the cavities are formed by different respective layers (40, 50) and first conductors (53) are disposed between the layers which form the backs of the cavities.

2. A device package as claimed in claim 1 wherein an array of internal terminals (28, 68) is peripherally disposed around each cavity, the second conductors (27, 67) each interconnect a contact pad (26, 66) of a semiconductor chip with an internal terminal, the first conductors each interconnect internal terminals or third conductors with other internal terminals or with other third conductors.

3. A device package as claimed in claim 1 or claim 2 wherein the external terminals comprise metallized areas disposed on the bottom horizontal surface of the chip carrier.

Patentansprüche

1. Halbleiterbauelementpackung, umfassend eine Chip-Träger (100) mit einem Paar Hohlräumen (21, 61), in denen je ein Halbleiterchip (25, 64) befestigt ist, wobei der Chip-Träger aufgebaut ist aus

— einer Vielzahl Schichten (10—90) aus isolierendem Material,

— horizontalen ersten Leitern (24, 53) auf einer horizontalen Fläche einer jeden von einer Mehrzahl der Schichten,

— zweiten Leitern (27, 67), die die Halbleiterchips mit bestimmten der ersten Leiter verbinden,

— einer Vielzahl vertikaler dritter Leiter (55), die sich je durch eine Mehrzahl der Schichten hindurcherstrecken, um erste Leiter verschiedener Schichten miteinander zu verbinden, und

— äußere Anschlüsse (93), die peripher an einer der Schichten befestigt sind, um selektiven elektrischen Kontakt zu den zweiten Leitern über die ersten und dritten Leiter zu ermöglichen,

dadurch gekennzeichnet, daß

— die Hohlräume (21, 61) innerhalb des Trägers Rückseite an Rückseite zueinander angeordnet sind,

— die Rückseiten der Hohlräume durch je verschiedene Schichten (40, 50) gebildet sind und

— erste Leiter (53) zwischen den die Rückseiten der Hohlräume bildenden Schichten angeordnet sind.

2. Bauelementpackung wie in Anspruch 1 beansprucht, wobei

— ein Feld innerer Anschlüsse (28, 68) in peripherer Anordnung um jeden Hohlraum herum vorgesehen ist,

When the series of ceramic members 10, etc., are sandwiched together and the via holes filled with the metallic paste, the assembly is fired to produce a unitary member comprising the double cavity semiconductor chip carrier. In the unitary assembly interconnections may be made from particular contact pads on each of the mounted semiconductor chips through the various metallization leads to terminate in certain of the external terminals 93 on the bottom face of the carrier. Interconnection between particular contact pads on the semiconductor chips also can be made. It will be evident that, in the typical instance, in which both semiconductor chips are of the integrated circuit type a considerable flexibility of interconnection is possible, even for a given design of carrier. In particular, computer programming can be used to determine the interconnection pattern for particular semiconductor devices which are paired in particular double cavity carriers of this general configuration. Within the general carrier configuration, as previously noted, various designs may be fabricated to have different interconnection arrangements. These different arrangements may be obtained by relatively simple variations in metallization masks and via patterns.

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— die zweiten Leiter (27, 67) je eine Kontaktstelle (26, 66) eines Halbleiterchips mit einem inneren Anschluß verbinden und

— die ersten Leiter je innere Anschlüsse oder dritte Leiter mit anderen inneren Anschlüssen oder mit anderen dritten Leitern verbinden.

3. Bauelementpackung wie in Anspruch 1 oder Anspruch 2 beansprucht, wobei

— die äußeren Anschlüsse metallisierte Gebiete umfassen, die auf der unteren horizontalen Fläche des Chip-Trägers angeordnet sind.

Revendications

1. Un boîtier de dispositif semiconducteur consistant en un support de puces (100) comprenant une paire de cavités (21, 61) dans chacune desquelles est montée une puce de semiconducteur (25, 64), le support de puces étant constitué par un ensemble de couches (10—90) de matière isolante, des premiers conducteurs horizontaux (24, 53) sur une surface horizontale de chaque couche d'un ensemble desdites couches, des seconds conducteurs (27, 67) interconnectant les puces de semiconducteur à certains des premiers conducteurs, un ensemble de troisièmes conducteurs verticaux (55), chacun d'eux traversant un ensemble des couches pour interconnecter des premiers conducteurs de différentes couches, et des bornes externes (93) montées à la périphérie de l'une des couches pour permettre un contact électrique sélectif avec les seconds conducteurs par l'intermédiaire des premiers conducteurs et des troisièmes conducteurs, caractérisé en ce que les cavités (21, 61) sont disposées dos à dos à l'intérieur du support, les fonds des cavités sont formés par différentes couches respectives (40, 50) et des premiers conducteurs (53) sont disposés entre les couches qui forment les fonds des cavités.

2. Un boîtier de dispositif selon la revendication 1, dans lequel un réseau de bornes internes (28, 68) est disposé à la périphérie de chaque cavité, chacun des seconds conducteurs (27, 67) interconnecte un plot de contact (26, 66) d'une puce de semiconducteur avec une borne interne, et les premiers conducteurs interconnectent respectivement des bornes internes ou des troisièmes conducteurs avec d'autres bornes internes ou avec d'autres troisièmes conducteurs.

3. Un boîtier de dispositif selon la revendication 1 ou la revendication 2, dans lequel les bornes externes sont constituées par des régions métallisées disposées sur la surface horizontale inférieure du support de puces.

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