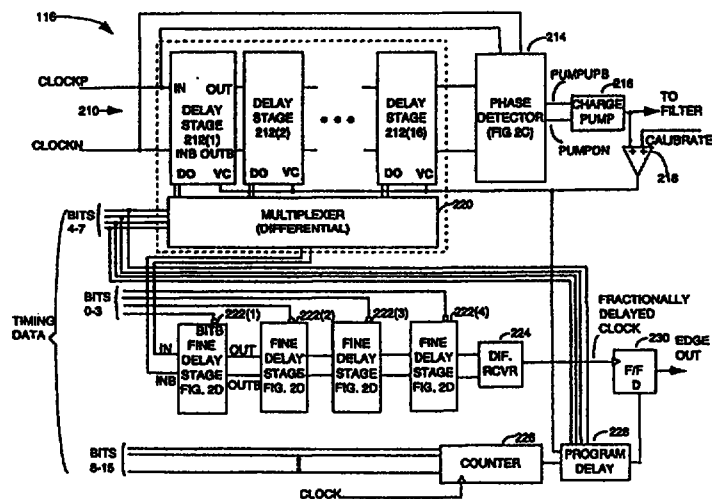




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(54) Title: **LOW COST CMOS TESTER**

(57) Abstract

Automatic test equipment implemented with low cost CMOS components. Despite the use of CMOS circuitry, which generally has poor timing accuracy, the disclosed test equipment achieves good timing accuracy through the use of several techniques. A delay locked loop is used to compensate for timing variations caused by process variation and slowly varying changes in operating temperature. A frequency dependent heating element is used to avoid temperature induced changes in propagation delays caused by rapid variations in the heat generated by the CMOS circuitry when the operating frequency changes. The design also reduces the number of circuit elements in the critical timing paths which process signals which vary with programmed frequency. To achieve this goal, a continuously running, fixed frequency reference clock is delayed by a fractional amount of one clock period. A counter, also clocked at the reference clock frequency, counts full clock periods. The number of full clock periods as well as the amount of fractional delay is programmed. When the required number of full clock periods has elapsed, the next pulse of the fractionally delayed clock signal is gated to the output of the timing generator as an edge signal with the programmed interval between pulses.

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