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(71) Applicant: INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95052 (US).

(72) Inventors: KARDACH, James; 541 Laswell Avenue, San Jose, CA 95128 (US). CHO, Sung, Soo; 1521 Jasper Drive, Sunnyvale, CA 94087 (US). PETERSON, Nicholas, B.; 704 Applause Place, San Jose, CA 95134 (US). LANE, Thomas, R.; 616 Chapman Street, San Jose, CA 95126 (US). JOSHI, Jayesh, M.; 510 Mansion Court #104, Santa Clara, CA 95054 (US). SONGER, Neil; 4281 Norwalk Drive #W106, San Jose, CA 95129 (US).

(74) Agents: MALLIE, Michael, J. et al.; Blakely, Sokoloff, Taylor & Zafman, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025-1026 (US).



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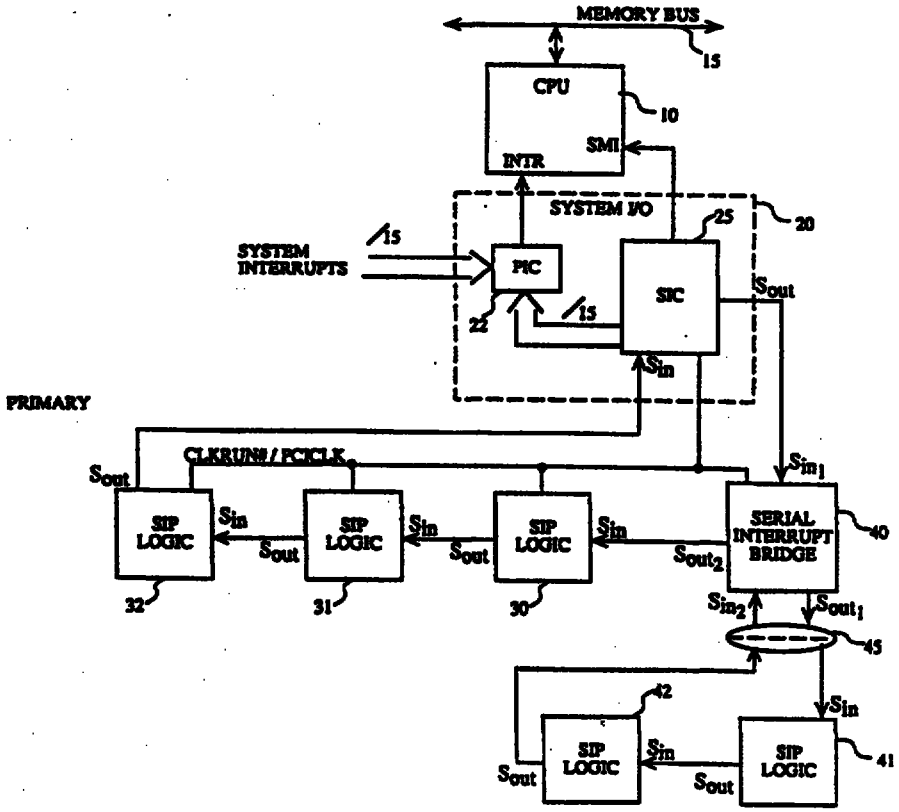
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(54) Title: SERIAL INTERRUPT BUS PROTOCOL


(57) Abstract

A serial interrupt bus protocol is implemented in which any number of peripherals in a computer system may signal any predetermined interrupt signals to the system's interrupt controller (22) without requiring a dedicated pin for each possible interrupt. Each peripheral implemented on the serial interrupt bus incorporates state machine logic for cycling through possible interrupt states. The peripherals are daisy chained beginning and ending with a serial interrupt controller (25) which follows the same state machine logic as the sytem peripherals. When the serial interrupt controller (25) receives an active signal, it determines which interrupt signal to provide to the system's interrupt controller (22) based on the interrupt state of the interrupt controller state machine logic. Peripherals (41, 42) on a secondary serial interrupt bus may be daisy chained with peripherals (30, 31, 32) on a primary system interrupt bus through a system interrupt bridge (40) which also includes state machine logic for following the same state diagram as the system peripherals.

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