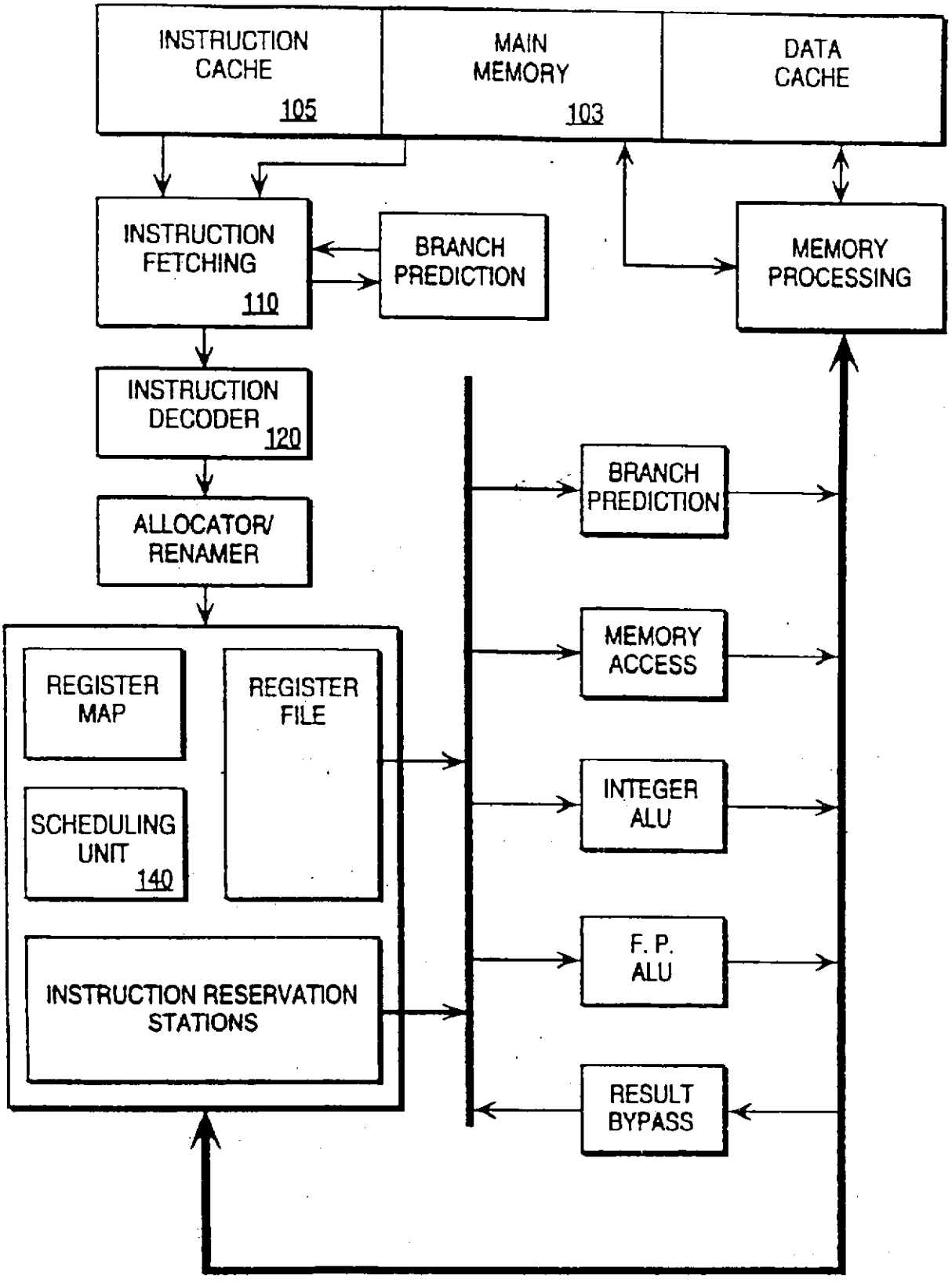


FIG. 1 (PRIOR ART)

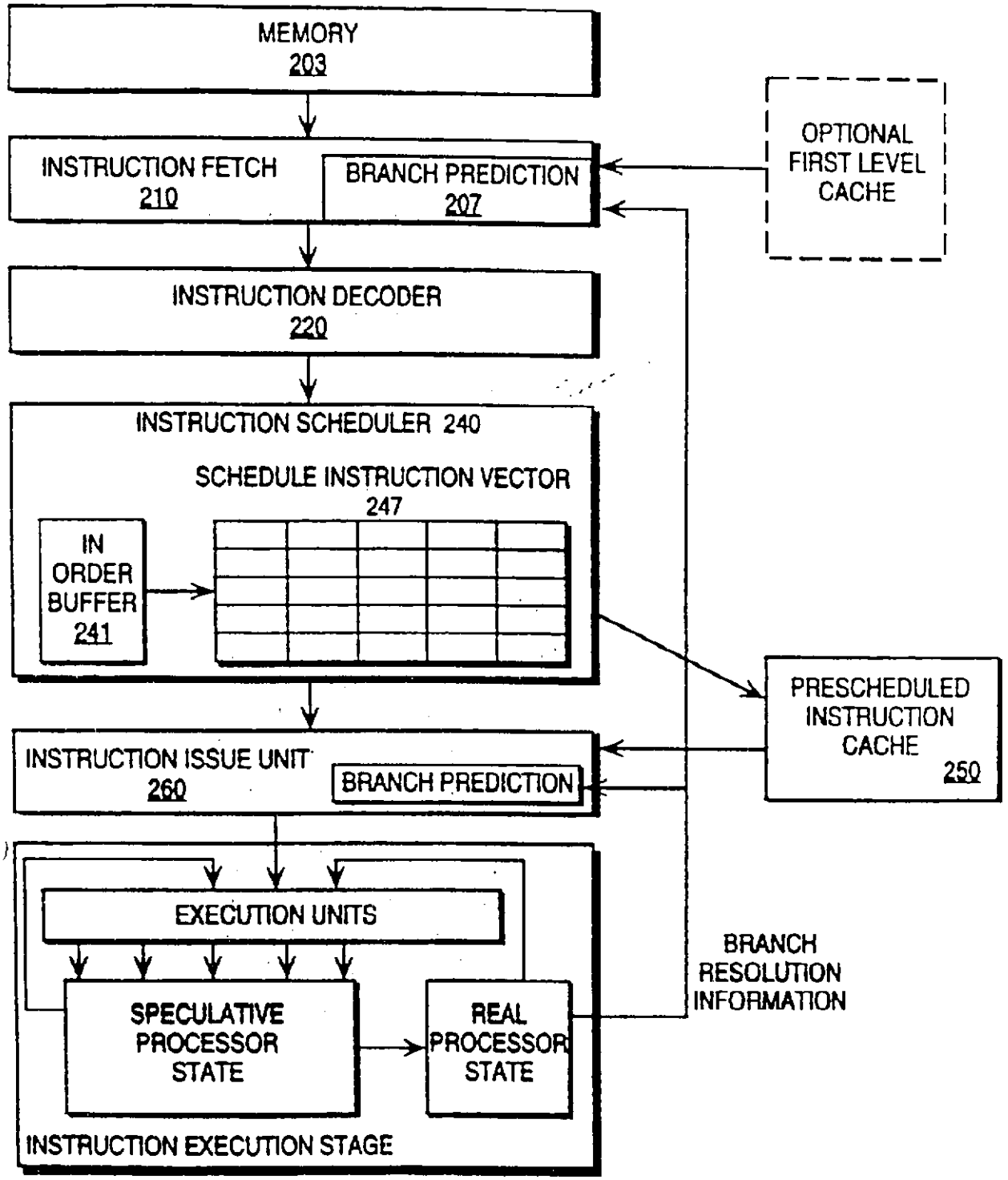

MEMORY
203
INSTRUCTION FETCH
210
BRANCH PREDICTION
207
OPTIONAL
FIRST LEVEL
CACHE
INSTRUCTION DECODER
220
INSTRUCTION SCHEDULER 240
SCHEDULE INSTRUCTION VECTOR
247
IN
ORDER
BUFFER
241
PRESCHEDULED
INSTRUCTION
CACHE
250
INSTRUCTION ISSUE UNIT
260
BRANCH PREDICTION
EXECUTION UNITS
SPECULATIVE
PROCESSOR
STATE
REAL
PROCESSOR
STATE
BRANCH
RESOLUTION
INFORMATION
INSTRUCTION EXECUTION STAGE

FIG. 2

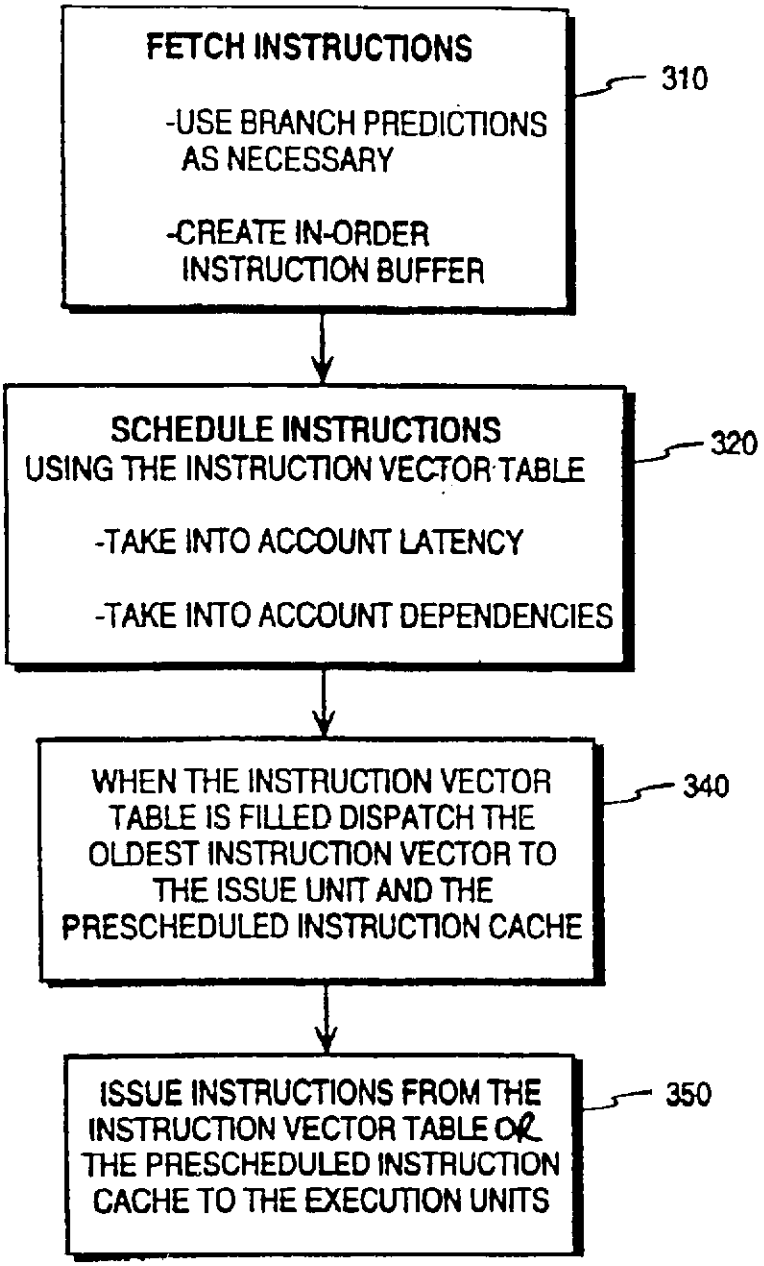

FETCH INSTRUCTIONS
-USE BRANCH PREDICTIONS AS NECESSARY
-CREATE IN-ORDER INSTRUCTION BUFFER
310
SCHEDULE INSTRUCTIONS USING THE INSTRUCTION VECTOR TABLE
-TAKE INTO ACCOUNT LATENCY
-TAKE INTO ACCOUNT DEPENDENCIES
320
WHEN THE INSTRUCTION VECTOR TABLE IS FILLED DISPATCH THE OLDEST INSTRUCTION VECTOR TO THE ISSUE UNIT AND THE PRESCHEDULED INSTRUCTION CACHE
340
ISSUE INSTRUCTIONS FROM THE INSTRUCTION VECTOR TABLE OR THE PRESCHEDULED INSTRUCTION CACHE TO THE EXECUTION UNITS
350

FIG. 3

EU1	EU2	EU3	EU4	EU5	WAIT	PC INCREMENT

FIG. 4A

INSTRUCTION	SOURCE 1 OPERAND	SOURCE 2 OPERAND	DESTINATION	RELATIVE PC

FIG. 4B

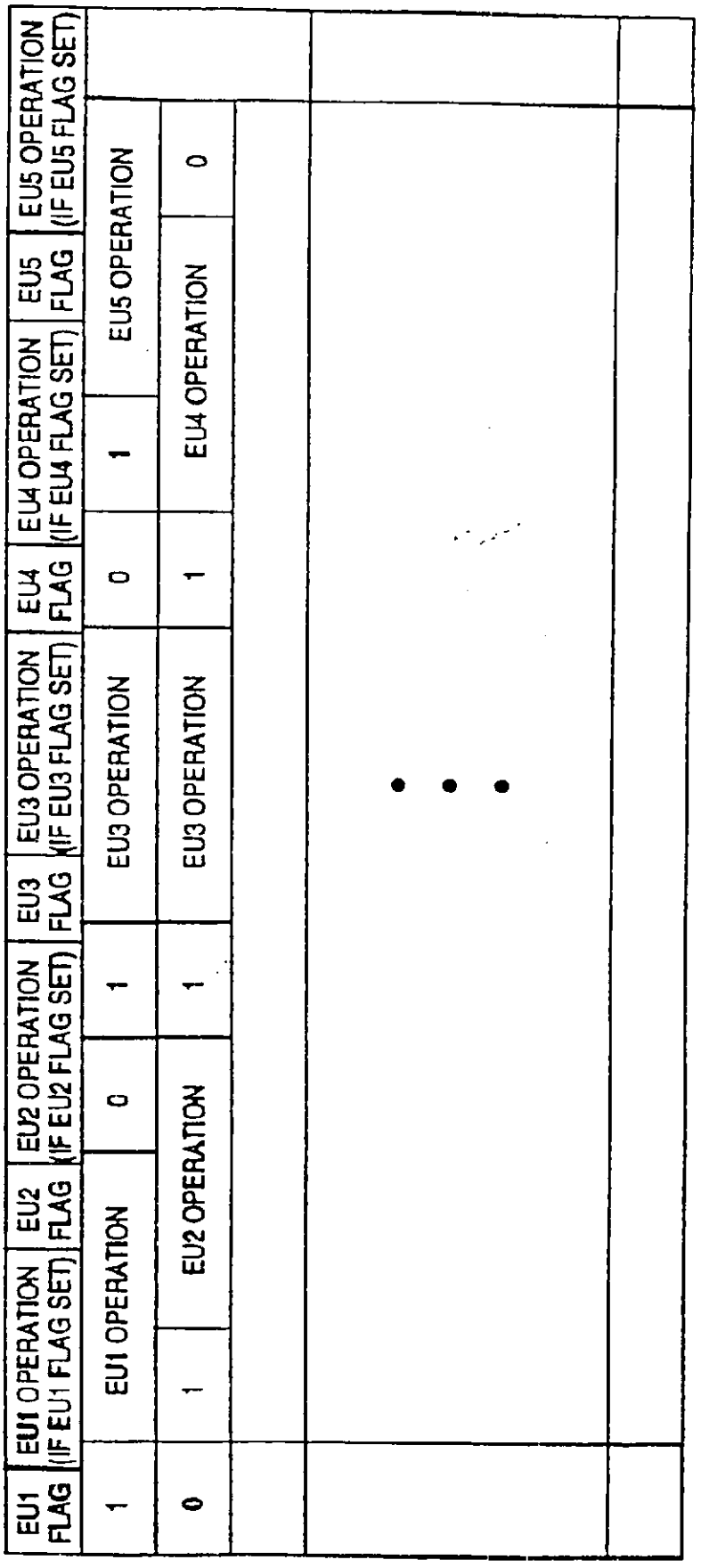

EU1 FLAG
EU1 OPERATION (IF EU1 FLAG SET)
EU2 FLAG
EU2 OPERATION (IF EU2 FLAG SET)
EU3 FLAG
EU3 OPERATION (IF EU3 FLAG SET)
EU4 FLAG
EU4 OPERATION (IF EU4 FLAG SET)
EU5 FLAG
EU5 OPERATION (IF EU5 FLAG SET)
1
EU1 OPERATION
0
1
EU3 OPERATION
0
EU5 OPERATION
0
1
EU2 OPERATION
1
EU3 OPERATION
1
EU4 OPERATION
0

FIG. 5

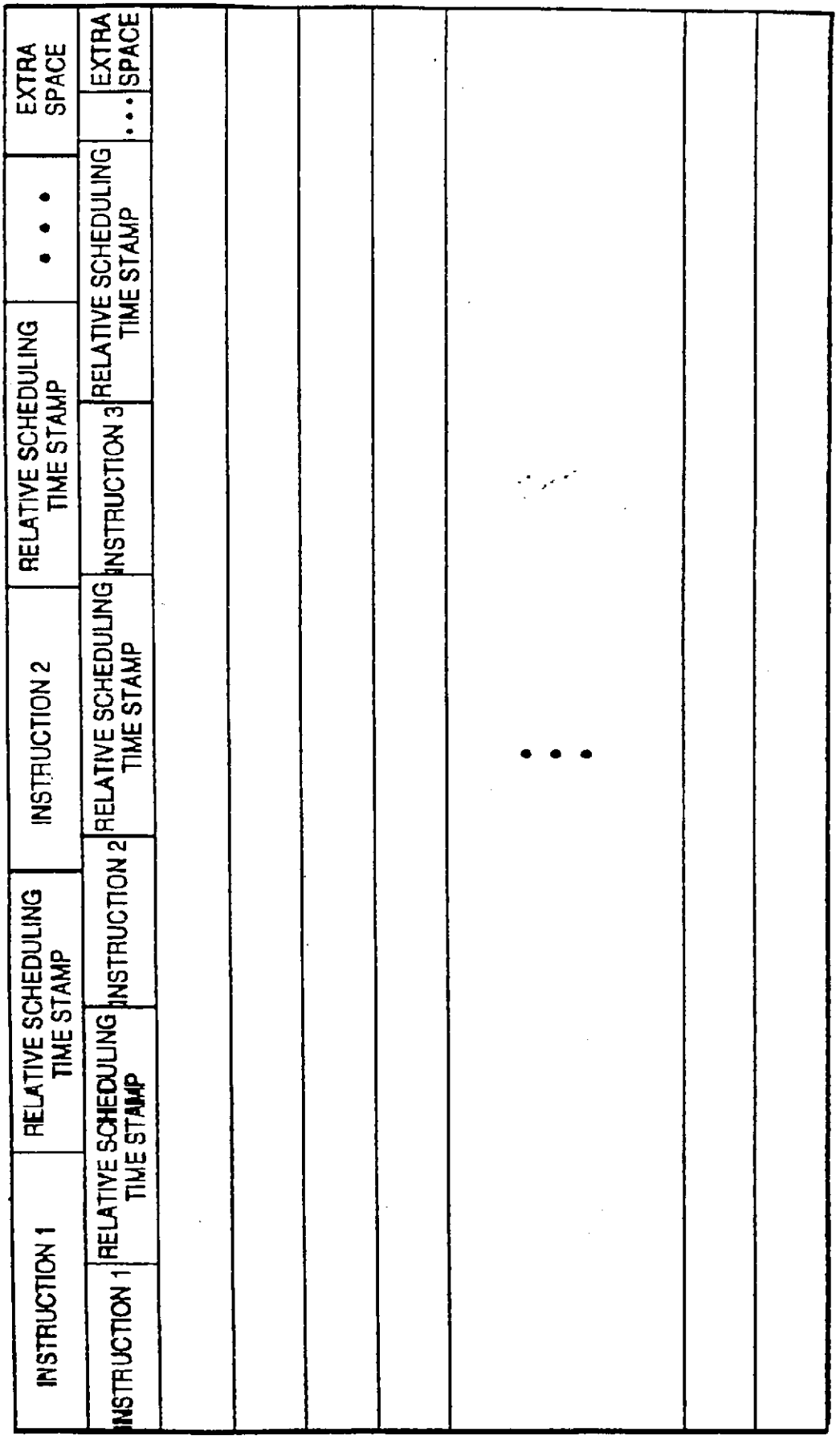

INSTRUCTION 1
RELATIVE SCHEDULING TIME STAMP
INSTRUCTION 2
RELATIVE SCHEDULING TIME STAMP
INSTRUCTION 3
RELATIVE SCHEDULING TIME STAMP
• • •
EXTRA SPACE
INSTRUCTION 1
RELATIVE SCHEDULING TIME STAMP
INSTRUCTION 2
RELATIVE SCHEDULING TIME STAMP
INSTRUCTION 3
RELATIVE SCHEDULING TIME STAMP
• • •
EXTRA SPACE

FIG. 6