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(71) Applicants: **ADVANCED MICRO DEVICES, INC.** [US/US]; One AMD Place, Mail Stop 68, Sunnyvale, CA 94088-3453 (US). **FUJITSU LIMITED** [JP/JP]; 1-1, Kamikodanaka 4-chome, Nakahara-ku, Kuwasaki-shi, Kanagawa 211 (JP).

(72) Inventors: **AL-SHAMMA, Ali**; 2966 Moorpark #10, San Jose, CA 95128 (US). **AKAOGI, Takao**; 7911 October Way, Cupertino, CA 95014 (US).

(74) Agent: **RODDY, Richard, J.**; Advanced Micro Devices, Inc., One AMD Place, Mail Stop 68, Sunnyvale, CA 94088-3453 (US).

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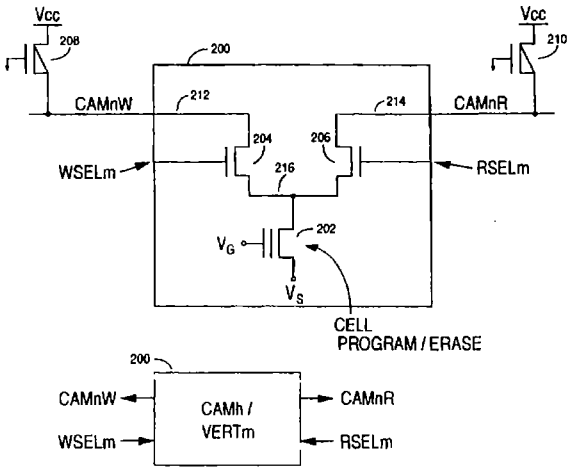
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(54) Title: BURST READ INCORPORATING OUTPUT BASED REDUNDANCY



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(57) Abstract: A device for performing redundant reading in a flash memory. The device includes arrays of regular memory cells (410) and arrays of redundant memory cells (412). Some of the regular memory cells may have defective addresses. A regular sense amplifier (420) will read the regular memory cells at their accessed address while a redundant sense amplifier (422) will read the redundant memory cells. A first array (432) of CAMs will store the defective addresses of the defective memory cells while a second array (432) of CAMs will store the input/output designators of the defective memory cells. Decoding circuitry (460) will decode the input/output designators of both the defective and non-defective memory cells A multi-bit multiplexer stage (490) will output either the contents of the regular memory cell (410) or, if the address is defective, the contents of the redundant memory cell (412). The contents will be applied to the multiplexer output corresponding to the input/output designator of the memory cell.

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