

PATENT SPECIFICATION

1,183,627

DRAWINGS ATTACHED.

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International Classification:—B 41 j 3/20.

COMPLETE SPECIFICATION.

High Speed Thermal Printer.

We, TEXAS INSTRUMENTS INCORPORATED, a Corporation organised according to the laws of the State of Delaware, United States of America, of 13500 North Central Expressway, Dallas, Texas, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates generally to thermal printing, and more particularly relates to a high speed thermal print head suitable for use as a readout system for digital data storage and processing systems, and the like.

There are a great many applications for high speed printing devices. For example, the speed of many computers and data handling systems is limited by the rate at which data can be read out in printed form. Similarly, the rate at which written and pictorial information can be transmitted between two remote points is limited by the rate at which the data can be reproduced in printed or pictorial form. In most data readout systems, the recording sheet is indexed past a printing station where the characters are formed on the paper either by mechanical impact or by a thermal or photographic printing process. The speed of operation of these systems is dependent to a large extent upon the rate at which the recording sheet can be indexed past the printing station, as well as the speed at which the printing station can be operated.

The present invention provides a thermal printing device having a rotatable drum on the surface of which is a matrix of controllable heating elements, a memory arrangement carried by, preferably within, the drum and which is capable of receiving

and storing serial data and of converting the stored serial data to parallel data at a plurality of parallel outputs from the memory arrangements, the parallel outputs being coupled to activate associated heating elements in accordance with the pattern of data at the respective outputs to produce corresponding patterns of heated elements during a selected portion of each revolution of the drum, and means operable to transfer the said serial data to the memory arrangement during a preceding portion of each revolution of the drum as the said associated heating elements are being rotated towards the said selected portion of that revolution. In operation of the device, a strip or sheet of thermally responsive material moves with the rotatable drum and is disposed adjacent the heating elements during the said selected portion of a revolution of the drum so that the pattern generated by the heated elements is transferred to the thermally responsive material.

The transfer means can comprise: means operable to transfer a data signal from a circuit external of the drum to a circuit rotating with the drum, a gating circuit carried by the drum for selectively routing the data signal to the memory arrangement when the gating circuit is enabled, and a synchronizing circuit carried by the drum which is operably responsive to the angular position of the drum to enable the gating circuit when the matrix is traversing the said preceding portion of each revolution of the drum. Suitably, the memory arrangement may comprise shift registers capable of receiving serial data and converting such data into parallel data appearing at parallel outputs from the shift registers.

In a particular embodiment, the matrix of

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controllable heating elements is divided into a plurality of sub-matrices spaced circumferentially around the drum and the memory arrangement comprises a plurality of portions, one for each sub-matrix. The parallel outputs of each memory portion are coupled to activate the heating elements of the associated sub-matrix in accordance with the data at the respective outputs of that memory portion and the transfer means is operable to transfer serial data to the respective portions of the memory arrangement in a predetermined sequence. Each portion of the memory arrangement can be divided into a plurality of sections, the transfer means then being arranged to supply serial data to each section of a portion of the memory arrangement over a different data channel.

A device in accordance with the invention can be constructed to process serial data and to print out such data in a variety of forms e.g. alphanumeric or pictorial, one particular application being to provide an alphanumeric readout for a digital computer. A device constructed in accordance with the invention may also be used to provide a readout device for large, high speed memories e.g. it may be used as a high speed facsimile printer or as a real time pictorial recorder for a television signal.

By way of example, embodiments of the invention will be described in greater detail with reference to the accompanying drawings in which:

Figure 1 is a schematic side view of a thermal printing device constructed in accordance with the present invention;

Figure 2 is a simplified sectional view taken generally on lines 2—2 of Figure 1;

Figure 3 is a schematic logic and circuit diagram of the thermal printing device of Figure 1;

Figure 4 is a simplified perspective view of a typical thermal print head used in the device of Figure 1;

Figure 5 is a simplified sectional view of the thermal print head of Figure 4;

Figure 6 is a schematic circuit diagram of a heater circuit of the thermal print head of Figure 4; and

Figure 7 is a schematic logic and circuit diagram of an alternative embodiment of a thermal printing device constructed in accordance with the present invention.

Referring now to the drawings, a thermal printing device constructed in accordance with this invention is indicated generally by the reference numeral 10 in the schematic illustration of Figure 1. The printing device 10 is comprised of a cylindrical drum 12 mounted on a rotating shaft 14. The shaft and drum are driven by some suitable means represented by the motor 16 at a pre-selected speed. As can be seen in Figure

2, a length of heat sensitive paper 18 passes around the cylinder 12 as the cylinder 12 rotates, and is in contact with the cylinder over approximately 180° of its circumference. The paper 18 may be either a continuous strip, or a series of sheets, and a suitable conventional means is provided to handle the paper.

The particular embodiment of the print head presently to be described is adapted to print lines of alphanumeric characters. This is accomplished by fifty thermal print heads P_1 — P_{50} which extend longitudinally of the drum 12 and are equally spaced around the periphery of the drum. Each of the fifty print heads P_1 — P_{50} is comprised of one hundred twenty alphanumeric character matrices C_1 — C_{120} (see Figure 3), and each of the character matrices is comprised of twenty-five individually controlled hot spots 20. Thus, as illustrated in the schematic logic diagram of Figure 3, character matrices C_1 — C_{120} of print head P_1 are designated as P_1C_1 — P_1C_{120} , the character matrices of print head P_2 are designated as P_2C_1 — P_2C_{120} , and finally the character matrices of the print head P_{50} are designated as $P_{50}C_1$ — $P_{50}C_{120}$. Thus, it will be noted that each of the print heads P_1 — P_{50} has three thousand individually controllable hot spots 20.

Each of the thermal print heads P_1 — P_{50} may be fabricated, for example, using the methods described in British Patent Specification No. 1,151,848. More particularly, each of the hot spots 20 may be comprised of a body 54 of semiconductor material (see Figure 5) covered by a layer of silicon carbide 57. The silicon carbide surface layer 57 is in direct contact with the paper 18 and provides a highly wear resistant surface. Each of the hot spots 20 is heated by a heater circuit, indicated generally by the reference numeral 56 in Figure 6, the components of which are formed by diffusion or other conventional techniques within the semiconductor bodies 54. The heater circuit 56 is comprised of transistors 58 and 60 and collector resistors 62 and 64, connected in the conventional manner illustrated. The base 66 of transistor 58 is the control input of the heater circuit. When a logic "0" level, i.e., 0.0 volt, is applied to terminal 66, the heater circuit is turned off. When a positive voltage representative of a logic "1" level is applied to the control terminal 66, transistors 58 and 60 conduct, and the current through the transistors and through the collector resistors heats the entire semiconductor body 54 and the overlying silicon carbide layer 57. The leads interconnecting the transistors and resistors of the heater circuit 56 and the input leads and voltage supplies for the various heater circuits of the matrix may be formed as first

and second formed on or fourth course, be thus far substrate 78, such as heat down the as representation 80 in F character P_1C_1 and raised bar 84 and c 57.

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and second layer interconnections 68 and 72 formed on oxide layers 70 and 74. Third or fourth level interconnections may, of course, be used if necessary. The structure thus far described is mounted on a ceramic substrate 76 by a suitable bonding material 78, such as epoxy. The leads to the various heater elements 56 may then extend down the edge of the ceramic substrate 76, as represented schematically by the structure designated with the reference character 80 in Figure 4. Each adjacent pair of character matrices, for example matrices P₁C₁ and P₁C₂, may be separated by a raised bar 82 formed by semiconductor body 84 and covered by the silicon carbide layer 57.

The print head illustrated in Figures 4, 5 and 6 may be fabricated by first etching out grooves in the surface of a semiconductor body to form mesas corresponding to the semiconductor bodies 54 and 84. This may be accomplished using conventional photolithographic etching techniques. Then the silicon carbide layer 57 is deposited over the surface of the mesas and the grooves. This may be accomplished using, for example, a mixture of toluene (C₇H₈) and silicon tetrachloride (SiCl₄) vapors with hydrogen gas as the carrier. These gases, in a typical ratio of about 0.87 mole per cent silicon carbide, 0.18 mole per cent toluene, and the remaining mole percentage hydrogen, are passed over the substrate which is located in a suitable heated furnace and maintained at a temperature of about 1080° C. Next, a layer of polycrystalline or amorphous silicon is deposited over the surface of the silicon carbide layer by the hydrogen reduction of silicon tetrachloride, for example. This layer is not illustrated in the drawings because it is used merely to lend structural rigidity during processing and is subsequently removed. The surface of the semiconductor starting material opposite from the bodies 54 is then removed by lapping and polishing down to the silicon carbide layer 57 previously formed in the grooves. This leaves single crystal semiconductor bodies 54 as islands at the surface of the amorphous silicon body, the silicon islands being isolated from the amorphous silicon body by the silicon carbide layer 57. The silicon carbide layer 57 serves to limit the depth of the lapping and polishing process and assures that the thickness of the semiconductor bodies 54 will be uniform, thus insuring uniform heating and cooling rates for all of the hot spots.

The transistors and resistors can then be fabricated in the exposed surface of the semiconductor bodies 54 using any standard fabrication technique, and the various lead patterns formed in one or more layers on the surface of the substrate. This structure

is then inverted and mounted on the ceramic substrate 76 using the bonding layer 78, after which the amorphous layer of silicon is removed from the silicon carbide layer by a suitable etchant, such as a mixture of hydrofluoric acid, nitric acid and acetic acid. During this step of the process, the silicon carbide layer 57 acts as an etch barrier to protect the underlying silicon bodies 54, and permit the amorphous silicon to be etched from the grooves between the various hot spots.

Referring once again to Figure 3, fifty shift registers DSR₁—DSR₅₀ are provided for the fifty print heads P₁—P₅₀, respectively. In order to have maximum flexibility, each shift register has a three thousand bit storage capacity, and each bit is connected to control one of the hot spots 20. The shift registers are serial-to-parallel data converters in that three thousand bits of binary data may be serially fed into each register, then the three thousand bits of data are stored and converted to three thousand parallel outputs to control the corresponding hot spots. When only alphanumeric information is to be printed by the device 10, only thirty or forty characters will need to be printed by each character matrix, and in these circumstances the number of bits in the shift registers DSR for each character can be reduced from twenty-five (i.e. one for each hot spot of a character matrix) to about six, as required to provide a different code combination for each different character, if an appropriate decoding circuit is included to convert each six bit binary code combination into a corresponding twenty-five bit code combination to control the hot spots of the character matrix in such a manner as to produce the limited number of characters.

The data shift registers DSR₁—DSR₅₀ are preferably located adjacent to the print heads P₁—P₅₀ substantially as illustrated in Figure 2. The shift registers DSR₁—DSR₅₀ may be fabricated as integrated circuits occupying about the same volume of space as the print heads P₁—P₅₀. However, it will be appreciated that as much space as is required within the interior of the drum may be used for the shift registers, ring counter and steering gates presently to be described.

Fifty data gates DG₁—DG₅₀ and fifty clock gates CG₁—CG₅₀ are sequentially enabled by the outputs from the fifty bits b₁—b₅₀ of a ring counter RC. The ring counter RC is clocked by a low speed clock pulse train applied through slip ring 22 on the shaft 14, the slip ring input being designated by the same reference character in both Figures 1 and 3. The frequency of the low speed clock pulse train is equal to the number of data shift registers DSR times

the speed of rotation of the drum 12. Thus, if the drum is rotated at fifty revolutions per second, the low speed clock would have a frequency of 2500 pulses per second. The output from the last bit b_{50} of the ring counter may be fed out through slip ring 24 for synchronization purposes. The outputs from bits b_1 — b_{50} of the ring counter RC sequentially enable input data gates DG_1 — DG_{50} , respectively, and high speed clock gates CG_1 — CG_{50} , respectively.

A high speed clock signal is applied to the rotating drum and then to an input of each of the clock gates CG_1 — CG_{50} through slip ring 26. The frequency of the high speed clock is at least equal to the product of the total number of storage bits in the fifty data shift registers DSR_1 — DSR_{50} and the speed of rotation of the drum 12, plus a slight margin to facilitate operation of the steering logic as will hereafter be described. Input data is applied to the inputs of data gates DG_1 — DG_{50} through slip ring 28. The input data is in serial binary form, and is synchronized with the clock pulses applied through slip ring 26. Thus, the data signal would be at either a logic "0" or a logic "1" level during each of three thousand clock pulses, depending upon the binary value of the bit. Each successive bit of data is introduced to one end of the shift register, then shifted through the remaining bits of the register. After the three thousandth clock pulse, each of the three thousand bits of the shift register has the appropriate output, and these outputs are fed in parallel to control the three thousand hot spots until new data is fed into the shift register.

Electrical power for all of the circuits is applied through slip rings 30 and 32, it being understood that the two slip rings are merely exemplary and that as many slip rings as required can be provided to supply voltage supplies of different levels.

A pair of timing disks 34 and 36 are mounted on the shaft 14 in order to sense the position and speed of the drum 12 as represented in Figure 1. Fifty permanent magnets may be spaced around the periphery of the disk 34 to induce fifty pulses in the pickup head 38 during each revolution of the drum 12, the magnets preferably being positioned to correspond to the position of the print heads P_1 — P_{50} , respectively. The pulse train produced by disk 34 and pickup head 38 may be used to either synchronize or derive the low speed clock pulses used to operate the ring counter RC. A single magnet may be provided on disk 36 for inducing a single pulse in pickup head 40 during each revolution of the drum 12. This pulse is used as a reference to determine the position of the drum 12, and from this pulse and the pulses from slip

ring 24, the operation of the ring counter RC is synchronized with the rotation of the drum. Thus, the magnet and pickup head may be located to produce a pulse when print head P_1 is in the position illustrated in Figure 2, for example, indicating that bit b_1 of the ring counter should have a logic "1" output to enable the gates DG_1 and CG_1 as will now be described.

The printing device 10 is made compatible with a source of data 44 by an interface 42. The data source may be any desired high speed memory, computer, or other data processing system. The interface 42 takes the data from the source 44 and puts it in digital form suitable for operating the printing device 10, and synchronizes the supply of data with the operation of the printing device. The interface may vary widely in design and construction, depending upon the nature of the data provided by the source, but performs the primary function of supplying the binary data to be recorded by each of the print heads to the appropriate print head as the print head passes through the data input arc 50 (see Figure 2). To this end, the interface may control the rotation of the drum as represented by line 46 extending to motor 16. Thus, the interface provides an input data signal in the form of three thousand bits of serial data synchronized with three thousand clock pulses within the desired interval, and insures that the operation of the ring counter is synchronous with the rotation of the drum so that the gates DG_1 to DG_{50} and CG_1 to CG_{50} are enabled at the appropriate time.

In the operation of the device 10, the drum 12 is rotated at some desired constant speed, such as fifty revolutions per second. The ring counter RC would then operate at a rate of twenty-five hundred counts per second. The count of the ring counter RC is synchronized with the position of the drum 12 so that the output from bit b_1 enables gates DG_1 and CG_1 during the period that print head P_1 passes through the input arc 50 equal to no more than one-fiftieth of one revolution. Then as print heads P_2 , P_3 , etc. successively pass through the arc 50, gates DG_2 and CG_2 , DG_3 and CG_3 , etc. are successively enabled by the output from bits b_2 , b_3 , etc. of the ring counter RC.

Coincident with the enabling of gates DG_1 and CG_1 , three thousand bits of serial binary data are introduced through slip rings 26 and 28 in the form of a data signal level synchronized with three thousand clock pulses. The serial data is then stored in data shift register DSR_1 and converted into parallel digital data to simultaneously control the three thousand hot spots 20 of print head P_1 and form the desired charac-

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ters within the one hundred twenty character matrices, P_1C_1 — $P_{120}C_{120}$. As the drum 12 continues to rotate, registers DSR_2 — DSR_{120} are sequentially loaded as they pass through the arc 50. During the period of time that the individual print heads rotate from the loading arc 50 into contact with the paper 18, the newly energized hot spots have time to heat up, and the newly de-energized hot spots have time to cool off. The print heads P_1 — P_{120} then successively engage the paper 18 and remain in contact with preselected positions on the paper as the drum and paper rotate through approximately 180° . The procedure is then repeated.

Thus, it will be noted that by using fifty print heads and a drum speed of fifty revolutions per second, twenty-five hundred lines per second are printed with each line containing one hundred twenty characters. Of course, this can be increased or decreased as desired by variations in the number of print heads and in the speed of rotation of the drum. The particular number of print heads and the particular speed of rotation was selected merely as exemplary, and the components herein described for accomplishing this rate are presently within the state of the art.

The rate at which the input data is supplied to the various data shift registers DSR_1 — DSR_{120} is rather high, being 7.5 million bits per second in the particular embodiment described. Thus, the shift register DSR_n must operate at a rather high frequency. An alternative embodiment of the invention in which the frequency of the input data is reduced is indicated generally by the reference numeral 100 in Figure 7. The printing device 100 is very similar to the printing device 10 and corresponding parts are therefore designated by corresponding reference numerals. The printing device 100 differs from the printing device 10 principally in that five shift registers, each having a six hundred bit capacity, are provided for each of the fifty print heads, rather than a single shift register having a three thousand bit capacity. Thus, data shift registers DSR_{11a} — DSR_{11e} control the individual hot spots of print head P_1 , data shift registers DSR_{2a} — DSR_{2e} control the individual hot spots of print head P_2 , etc. The shift registers DSR_{1a} — DSR_{1e} are simultaneously loaded with data through slip rings 102—106 and data gates DG_{1a} — DG_{1e} when the gates are enabled by an output from bit b_1 of the ring counter RC. Similarly, shift registers DSR_{2a} — DSR_{2e} are simultaneously loaded through gates DG_{2a} — DG_{2e} when bit b_2 of the ring counter RC has a logic "1" output. Clock gate CG_1 gates the clock pulse train to all five of the shift registers DSR_{1a} — DSR_{1e} , and clock gate CG_2 gates

the clock pulse train to registers DSR_{2a} — DSR_{2e} , etc.

The operation of the printing device 100 is identical to the operation of the device 10 except that the serial binary input data to each of the five shift registers for each of the print heads is loaded simultaneously, i.e., in parallel, from the five separate slip rings and the gates DG_{1a} to DG_{1e} , DG_{2a} to DG_{2e} , etc. so that the rate at which the data is put into the individual storage means, and thus the rate at which the shift registers must operate, is reduced by one-fifth. It will readily be evident that the number of shift registers for each print head may be increased or decreased to decrease or increase, respectively, the rate at which data is serially put into the individual shift registers. Thus, in the printing device 100, the data is provided at a rate of 1.5 million bits per second as opposed to 7.5 million bits per second in the printing device 10.

Although the embodiments of the invention herein described have been specifically directed toward printing lines having one hundred twenty alphanumeric characters, it is to be understood that substantially any type of data may be printed in accordance with the broader aspects of the invention. For example, the entire surface of the drum may form a single matrix of hot spots. The matrix may be divided in a convenient manner into two or more sections and one or more shift registers provided for each section. The shift registers for the matrix sections may then be sequentially loaded during the portion of the revolution that the matrix section is not contacting the paper. In the event a plurality of shift registers are used to control each matrix section, the shift registers can be loaded in parallel.

From the above detailed description of the invention, it will be noted that an extremely high speed printer has been described. The printing device is compatible with high speed data processing systems and can be used at the data readout for such systems. The printing device can be used as a high speed facsimile readout device. By way of example, the device herein described has sufficient speed capability to record, in real time, the successive frames of conventional television transmission.

WHAT WE CLAIM IS:—

1. A thermal printing device having a rotatable drum on the surface of which is a matrix of controllable heating elements, the drum carrying a memory arrangement capable of receiving and storing serial data and of converting the stored serial data to parallel data at a plurality of parallel outputs from the memory arrangements, the parallel outputs being coupled to activate associated heating elements in accordance

ters within the one hundred twenty character matrices, P_1C_1 — $P_{12}C_{12}$. As the drum 12 continues to rotate, registers DSR_1 — DSR_{50} are sequentially loaded as they pass through the arc 50. During the period of time that the individual print heads rotate from the loading arc 50 into contact with the paper 18, the newly energized hot spots have time to heat up, and the newly de-energized hot spots have time to cool off. The print heads P_1 — P_{50} then successively engage the paper 18 and remain in contact with preselected positions on the paper as the drum and paper rotate through approximately 180° . The procedure is then repeated.

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From the above detailed description of the invention, it will be noted that an extremely high speed printer has been described. The printing device is compatible with high speed data processing systems and can be used at the data readout for such systems. The printing device can be used as a high speed facsimile readout device. By way of example, the device herein described has sufficient speed capability to record, in real time, the successive frames of conventional television transmission.

WHAT WE CLAIM IS:—

1. A thermal printing device having a rotatable drum on the surface of which is a matrix of controllable heating elements, the drum carrying a memory arrangement capable of receiving and storing serial data and of converting the stored serial data to parallel data at a plurality of parallel outputs from the memory arrangements, the parallel outputs being coupled to activate associated heating elements in accordance



with the pattern of data at the respective outputs to produce corresponding patterns of heated elements during a selected portion of each revolution of the drum, and means operable to transfer the said serial data to the memory arrangement during a preceding portion of each revolution of the drum as the said associated heating elements are being rotated towards the said selected portion of that revolution.

2. A device according to Claim 1, wherein the memory arrangement is carried by and within the drum.

3. A device as claimed in Claim 1 or Claim 2, wherein the transfer means comprises: means operable to transfer a data signal from a circuit external of the drum to a circuit rotating with the drum, a gating circuit carried by the drum for selectively routing the data signal to the memory arrangement when the gating circuit is enabled, and a synchronizing circuit carried by the drum which is operably responsive to the angular position of the drum to enable the gating circuit when the matrix is traversing the said preceding portion of each revolution of the drum.

4. A device as claimed in Claim 1, wherein the matrix of controllable heating elements is divided into a plurality of sub-matrices spaced circumferentially around the drum and wherein the memory arrangement comprises a plurality of portions, one for each sub-matrix, the parallel outputs of each memory portion being coupled to activate the heating elements of the associated sub-matrix in accordance with the data at the respective outputs of that memory portion, and wherein the transfer means is operable to transfer serial data to the respective portions of the memory arrangement in a predetermined sequence.

5. A device as claimed in Claim 4, wherein each portion of the memory arrangement is divided into a plurality of sections, and the said transfer means supplies the serial data to each section of a portion of the memory arrangement over different data channels.

6. A device as claimed in Claim 4, wherein each portion of the memory arrangement comprises a shift register capable of receiving serial data and storing such data as parallel data appearing at parallel outputs from that shift register.

7. A device as claimed in Claim 6, wherein the shift registers are carried within the drum, each shift register being disposed radially inwardly of its associated sub-matrix.

8. A device as claimed in Claim 6 or Claim 7, wherein the sub-matrices and the associated shift registers are constructed in semiconductor integrated circuit network form.

9. A device as claimed in any of Claims 6, 7 and 8, wherein the transfer means comprises: for each shift register a separate data gate carried by the drum, each data gate being connected to supply a data signal to the respective shift register when enabled; an input circuit carried by the drum for receiving data signals from a source external of the drum and applying such data signals to each of the data gates; for each shift register, a clock gate carried by the drum, each clock gate being connected to supply, when enabled, a clock pulse train to the associated shift register; a control circuit carried by the drum for receiving a clock pulse train synchronized with the data signals from a source external of the drum and for applying the clock pulse train to each of the clock gates; and a synchronization circuit carried by the drum and connected to enable selectively each of the data and clock gates, the synchronization circuit being operable, in response to a synchronization signal related to the rotational position of the drum, to enable the data and clock data related to a particular sub-matrix as that sub-matrix passes through the said preceding portion of the revolution of the drum.

10. A device as claimed in any of Claims 4—9, wherein each sub-matrix comprises a row of character matrices each of which is capable, when activated, of producing alphanumeric characters.

11. A thermal printing device including a rotatable drum having disposed at circumferentially spaced locations around the periphery thereof, rows of matrices each comprising controllable heating elements; each matrix having associated therewith a set of shift registers carried by the drum, each shift register being capable of receiving serial data and storing such data as parallel data appearing at parallel outputs from that shift register, the outputs of the shift registers of each set being coupled to the heating elements of respective sections of the associated matrix to activate those elements in a manner determined by data at the parallel outputs, to produce selected patterns of heated elements in that associated matrix; the drum carrying a set of data gates for each set of shift registers, each data gate of a set being connected to supply, when enabled, a data signal to one of the shift registers of the associated set; a set of input circuits carried by the drum, each input circuit being connected to apply a data signal received from a source external of the drum, to one data gate of each set of data gates; a clock gate carried by the drum for each set of shift registers, each clock gate being connected to supply, when enabled, a clock pulse train to each shift register of the associated set of shift registers; a control

circuit carrying a clock pulse train to each of the data gates; a synchronization circuit carried by the drum and connected to enable selectively each of the data and clock gates, the synchronization circuit being operable, in response to a synchronization signal related to the rotational position of the drum, to enable the data and clock data related to a particular sub-matrix as that sub-matrix passes through the said preceding portion of the revolution of the drum.



Claims
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circuit carried by the drum for receiving a clock pulse train from a source external of the drum and for applying the clock pulse to each of the clock gates; and a synchronization circuit carried by the drum, the synchronization circuit being adapted to receive a synchronization signal related to the rotational position of the drum from a source external of the drum and, in response to the synchronization signal, selectively to enable the clock gate and the set of data gates related to each matrix as that matrix travels through the said preceding portion of the revolution of the drum.
12. A device as claimed in Claim 10, wherein each matrix row comprises a

plurality of character matrices each of which is capable, upon activation, of producing alphanumeric characters.
13. A thermal printing device substantially as described herein with reference to and as illustrated by Figures 1-6 of the accompanying drawings.
14. A thermal printing device substantially as described herein with reference to, and as functionally illustrated by, Figure 7 of the accompanying drawings.

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