



Receiver Structure for TD-SCDMA Downlink in a Fast Moving Environment

Field of the invention

- 5 The present invention provides a method and system for a TD-SCDMA downlink for use when the receiver is located in a fast moving environment, the method and system employing a novel receiver structure.

Background of the invention

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TD-SCDMA (Time Division Synchronous Code Division Multiple Access) is the Chinese contribution to the international family of Mobile Radio Systems for 3rd Generation. It was accepted by 3GPP in March 2001 as the low chip rate version of UMTS TDD. TD-SCDMA is able to support all 3G services from 8 kbps speech
15 services up to 2 Mbps packet data service with adapted optimum resource allocation.

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In TD-SCDMA, the frame length is 10ms, and each 10ms frame is divided into 2 sub-frames of 5ms. Each sub-frame consists of 7 slots and each slot is assigned
either to uplink or to downlink [1] [2]. The slot structure of the TD-SCDMA is shown in Figure 1 of the accompanying drawings, where it is shown that there are two data parts in each slot, each data part has 352chip. Two data parts are separated by 144 chips midamble, which is used for channel estimation. A conventional receiver for a CDMA system is a Rake receiver. However, due to
25 multiple access interference (MAI), the performance of a Rake receiver degrades as the number of simultaneous active code channel in the same slot increases. Therefore, the Rake receiver is not suitable for the TD-SCDMA.

An optimum multiuser detector consists of a bank of conventional single-user matched filters followed by application of the Viterbi algorithm. However its complexity grows exponentially as the number of user increases. To reduce this complexity, various sub-optimum detectors have been developed. In [3], Block
 5 Linear Equalization (BLE) or Joint Detection (JD) has been proposed for burst TDD-CDMA signals. Furthermore, for downlink signals, this algorithm can further be simplified into the so called SUD-BLE [4]. For the implementation of SUD-BLE, FFT algorithm [5, 6] can be adopted, thus greatly reducing the receiver complexity.

10 SUD-BLE is much simpler than JD when the FFT algorithm is adopted. But JD provides better performance than SUD-BLE when the spreading codes of other user are ideally known. In other words, JD needs *a-priori* knowledge of the spreading codes of the other users whilst SUD-BLE does not need this
 15 information. In TD-SCDMA, the base station does not transmit such information to the users, and user equipment need to perform active code detection. Active code detection not only increases the complexity of user equipment, but also degrades the performance of JD when incorrect spreading code is detected or mis-detected some active codes. Therefore, when TX diversity is not applied,
 20 only SUD-BLE need be considered .

Since in TD-SCDMA, the data symbols for each data part comprise 352 chips, the straightforward method for implementing a SUD-BLE is to use 512 FFT. However, when using 512 FFT, channel estimation obtained through midamble is
 25 used for the detection of whole data blocks (352 chips).

In the previously proposed method of TD-SCDMA downlink, the base station transmits a number of K data vectors $d(k)$, $k=1, \dots, K$, with each data vector for each code channel. Before transmission over the mobile radio channel, spectrum

spreading is performed by multiplying each data vectors with the user-specific (consisting of channelization code and scrambling code in TD-SCDMA) $c^{(k)}$, $k=1, \dots, K$. The transmitted signal by the base station is the superposition of K signal contributions. The transmitted signal propagates through a same channel with a
 5 discrete-time channel impulse response h characterizing the link between the base station and the mobile station. Thus, let

$$d(k) = (d_1^{(k)}, d_2^{(k)}, \dots, d_N^{(k)})^T, \quad k = 1, \dots, K \quad (1)$$

denotes the data transmitted by each user, consisting of N symbols.

Let

$$10 \quad h = (h_1, h_2, \dots, h_W)^T, \quad k = 1, \dots, K \quad (2)$$

represents the channel impulse response, with the impulse length of W chips,

Let

$$c^{(k)} = (c_1^{(k)}, c_2^{(k)}, \dots, c_Q^{(k)})^T, \quad k = 1, \dots, K \quad (3)$$

denotes the user k spreading sequence, with spreading factor of Q .

15 The received signal e can be written as follows (There are two such vectors received per timeslot)

$$e = (e_1, e_2, \dots, e_{NQ+W-1})^T = H C d + n = H S + n \quad (4)$$

Where,

$n = (n_1, n_2, \dots, n_{NQ+W-1})^T$ denotes the additive Gaussian noise sequence which
 20 represents the intercell interference and thermal noise , with zero mean and covariance matrix $R_n = E(n n^H)$.

$d = (d(1)^T, d(2)^T, \dots, d(K)^T)^T$, is the combined sequence of all the users data.

$S = C d = (S_1, S_2, \dots, S_{NQ})^T$ is the superposition of all K users.

$H = (H_{m,n})_{(NQ+W-1) \times NQ}$ is the channel impulse response matrix, and is a circulant
 25 matrix, and its elements relates to h vector through the following equation:

$$H_{m,n} = \begin{cases} h_{m-n+1} & \text{for } 1 \leq m-n+1 \leq W \\ 0 & \text{else} \end{cases} \quad (5)$$

$C = (C_{ij})_{NQ \times KN}$ is the spreading code matrix, and contains the user-specific codes ,

$$C_{Q(n-1)+q, n+N(k-1)} = \begin{cases} c_q^{(k)} & \text{for } k=1, \dots, K, n=1, \dots, N, q=1 \dots Q \\ 0 & \text{else} \end{cases} \quad (6)$$

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For convenience, the special case of the covariance matrix R_n of the noise vector being equal to $\sigma^2 I$ with I the identity matrix and σ^2 the variance of the each noise component, is considered.

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Based on MMSE criterion, the continuous-valued estimation of S can be written as:

$$\hat{S} = (\hat{H}^H \hat{H} + \sigma^2 R_s^{-1})^{-1} \hat{H}^H e \quad (7)$$

15 where, $R_s = E\{SS^H\}$ of dimension $NQ \times NQ$ is the covariance matrix of the sum vector S . $\hat{H}$ is the estimation of the H matrix. Implementation of R_s can be approximated by $R_s = I$. $(.)^H$ denotes the complex conjugation and transposition (Hermitian transposition)

20 For the description of the despreader or code-matched filter, the matrix

$$C^k = (C_{ij}^k)_{NQ \times N}, \text{ and}$$

$$C_{Q(n-1)+q, n}^k = \begin{cases} c_q^{(k)} & \text{for } n=1, \dots, N, q=1 \dots Q \\ 0 & \text{else} \end{cases} \quad (8)$$

is defined. The continuous-valued estimate of $d(k)$ after code matched filtering becomes:

$$\hat{d}(k) = (\text{diag}(C^{kH} C^k))^{-1} C^{kH} \hat{S} = \frac{1}{Q} C^{kH} \hat{S} \quad (9)$$

Considering that the H matrix is circulant, channel equalization can be performed efficiently in frequency domain, and estimation of S can be calculated as follows:

$$z = \frac{FFT^*(\hat{h})FFT(e)}{FFT^*(\hat{h})FFT(\hat{h}) + \sigma^2} \quad (10)$$

and

$$\hat{S} = IFFT(z) \quad (11)$$

10 where $\hat{h}$ is the estimation of the H matrix.

In TD-SCDMA, the maximum length of delay spread is $w=16$. Since the length of e is $352+16-1=367$, 145 zeros are padded before 512 FFT is applied to e . Since length of h is 16, 496 zeros are padded before 512 FFT applied to h . The diagram of 512 FFT is shown is Figure.2. Using (10), the z vector of length 512 is obtained, and estimation of S is obtained by performing 512 IFFT on z and discarding end 160 points to obtain 352 point.

A receiver architecture has been proposed, which uses an overlap-and-save 64 FFT/IFFT instead of 512 FFT [6] for fast moving environment. By adopting this structure, channel estimation tracking can be integrated into data detection due to subblock-processing.

For sub-block processing, firstly, 33 zeros are padded to the received signal e , and signal e is divided into 8 sub-blocks, each sub-block of length 64 chip, and between adjacent blocks, there are 16 chips overlap. The detailed overlapping of sub-block is shown in Figure 3. Let $e^{(j)}$ represent the data for sub-block j , $j=1, \dots, 8$.

Let estimation of channel impulse response for sub-block j be denoted as $h^{(j)}$, $j=1, \dots, 8$. Then the processing can be described as:

1) Calculating vector $g^{(j)}$ of dimension 64 according to (10) and (11):

$$5 \quad g^{(j)} = IFFT\left(\frac{FFT^*(h^{(j)})FFT(e^{(j)})}{FFT^*(h^{(j)})FFT(h^{(j)}) + \sigma^2}\right)$$

2) Estimation of $S^{(j)}$ is obtained by discarding the last 16 items or 48 items of $g^{(j)}$:

$$\hat{S}^{(j)} = \begin{cases} g^{(j)}(1:48) & 1 \leq j \leq 7 \\ g^{(j)}(1:16) & j = 8 \end{cases}$$

Where, $g(m:n)$ denotes taking the element of g with index from m to n .

10 The detailed architecture of overlap and save 64 FFT receiver is shown in Figure 4.

There are two problems with such prior art systems.

15 First, when using 512 FFT, channel estimation obtained through midamble is used for the detection of whole data blocks (352 chips). The prerequisite of such processing is that the channel variation during the whole data block shall not be significant. If the receiver is stationary or is located in a relatively slow moving environment, this condition can be fulfilled. In fast moving environment this
20 condition can not be fulfilled due to dramatic variation of channel coefficients. In a fast moving environment, if the channel variation is not tracked and further integrated into data detection part, the performance will be greatly degraded.

Overlap and save 64 FFT presents a second problem, namely that due to the
25 interference between adjacent blocks, and the interference from unwanted chips

in the same sub-block, the performance of such a receiver is interference limited and the BER performance shows a BER floor in the high SNR zone.

Summary of the invention

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To improve the performance of sub-block processing, the present invention defines a novel receiver structure for TD-SCDMA downlink for use in a fast moving environment such as a motor vehicle or train, when transmit diversity is not applied. In this structure, after first sub-block processing, the structure
10 regenerates the interference caused by adjacent blocks and unwanted chips in the same sub-block, and subtracts the interference from the received data signal. Then a second sub-block processing step is performed to detect data. Simulation studies have shown that this receiver structure provides a great improvement compared with conventional sub-block processing.

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Thus, a first aspect of the present invention provides a method of interference reduction in a TD-SCDMA downlink receiver, the method comprising partitioning a received signal into a number of sub-blocks of length N_T with an overlap length N_Z between adjacent sub-blocks and processing said sub-blocks so that
20 substantially only $M = N_T - N_Z$ is extracted as the desired data signal.

A second aspect of the present invention provides a TD-SCDMA downlink receiver comprising as interference reduction means, means for partitioning a received signal into a number of sub-blocks of length N_T with an overlap length
25 N_Z between adjacent sub-blocks and means for processing said sub-blocks so that substantially only $M = N_T - N_Z$ is extracted as the desired data signal.

Detailed Description of the Invention

In preferred embodiments, the overall sub-block processing comprises:

- 5 (a) applying a first sub-block processing operation to a received data signal;
- (b) for each sub-block of the received data signal, regenerating interference
 caused by adjacent blocks and unwanted chips in the same sub-block;
- 10 (c) subtracting the regenerated interference from said received data signal to
 generate a reduced interference data signal; and
- (d) applying a second sub-block processing operation to said reduce
 interference data signal.

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In fast moving environment, in order to track the channel variation, channel estimation tracking needs to be integrated into data detection. This has been found to necessitate sub-block processing.

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The difference between the method of the invention and the traditional Decision Feedback Equalization (DFE) is that: 1) traditional DFE is a single user detector, only one user is detected, while the method of the present invention works in a multiuser situation, K user or codes are detected at the same time. 2) with
25 traditional DFE feedback, every detected data symbol cancels its effect in the received signal but for the method of the invention, only the feedback part of (i.e. some, not all) of the detected data symbols is used for the cancellation of the interference caused by them.

The difference between the method and system of the present invention and Block Decision Feedback Equalization (BDFE) is that: 1) BDFE needs to perform matrix factorization, which is rather complex, while the method of the invention only performs FFT, which is much simpler. 2) with BDFE feedback, every
5 detected data symbol cancels its effect, while the method of the invention only uses the feedback part of (not all) the detected data symbols for the cancellation of the interference caused by them.

The difference between the method and system of the present invention and the
10 multistage SIC (Successive Interference Cancellation) or PIC (Parallel Interference Cancellation) is that traditional SIC or PIC applies a matched filter (or Rake receiver) to detect data symbols followed by regeneration of the interference caused by all of the data symbols. The present invention applies an equalizer to detect data symbols and only uses part of (i.e. some, not all) the
15 detected symbols to regenerate the interference.

Brief description of the Drawings

The present invention will now be explained in more detail by way of the following
20 Description of a preferred embodiment and with reference to the accompanying drawings, in which:

Figure 1 shows the burst structure for TD-SCDMA traffic slot;

25 Figure 2 shows the SUD_BLE using 512 FFT of prior art 1;

Figure 3 shows the diagram of overlapping for sub-block processing of prior art;

Figure 4 shows the overlap and save 64 FFT architecture of prior art;

Figure 5 shows diagram of the receiver structure of invention;

5 Figure 6 shows interference caused by sub-block processing;

Figure 7 shows BER comparison between conventional sub-block processing and novel sub-block processing, according to the present invention, for channel A, 120km/hr (3 equal power path, relative path delay is 0, 5chips, 10 chips);

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Figure 8 shows BER comparison between conventional sub-block processing and novel sub-block processing, according to the present invention, for channel A, 250km/hr (3 equal power path, relative path delay is 0, 5chips, 10 chips);

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Figure 9 shows BER comparison between conventional sub-block processing and novel sub-block processing, according to the present invention, for channel B, 120km/hr (4 path, relative power is (0 dB, -3 dB, -6 dB, -9 dB); relative path delay is 0, 1chips, 2 chips, 3 chips));and

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Figure 10 shows BER comparison between conventional sub-block processing and novel sub-block processing, according to the present invention, for channel B, 250km/hr (4 path, relative power is (0 dB, -3 dB, -6 dB, -9 dB); relative path delay is 0, 1chips, 2 chips, 3 chips)).

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Description of Preferred Embodiments

Conventional sub-block processing (Figure 4) suffers from the interference between adjacent blocks and unwanted chips in the same sub-block, therefore the performance of such a structure is interference limited and the BER performance shows a BER floor.

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In an embodiment of the present invention, in order to improve the performance of sub-block processing shown in Figure 4, a structure is used whereby length 64 FFT/IFFT sub-block processing, with 16 chips overlapping between adjacent blocks, is employed. After first sub-block processing, we regenerate the interference caused by adjacent blocks, and this interference is subtracted from the received data signal. Then a second sub-block processing is performed to detect data. The diagram is shown in Figure 5.

Firstly, after padding 33 zeros, the received signal $\mathbf{e}$ is divided into a number of 8 blocks with each sub-block 64 chips and 16 chips overlapping between adjacent blocks. By introducing sub-block processing, the channel can be assumed piecewise stationary within each sub-block. Then the Channel Impulse Response (CIR) within a sub-block is approximately equal to the CIR in the centre of the block. In the following description, it is presumed that $W = 16$. Further, no knowledge is assumed of the code sequence of all users.

After padding zero, the received signal vector of length 400 can be written as:

$$\mathbf{e}' = (e_1, e_2, \dots, e_{367}, \underbrace{0, \dots, 0}_{33 \text{ zeros}})^T \quad (12)$$

Let CIR in the centre of i th ($i = 1, \dots, 8$) sub-block be expressed as:

$$\mathbf{h}^{(i)} = (h_1^{(i)}, h_2^{(i)}, \dots, h_w^{(i)})^T, \quad k = 1, \dots, K \quad (13)$$

Let $e^{(i)}$ represent the received signal for i th ($i = 1, \dots, 8$) sub-block, which can be expressed as:

$$e^{(i)} = (e'_{(i-1)M+1}, e'_{(i-1)M+2}, \dots, e'_{(i-1)M+64})^T = H^{(i)}S^{(i)} + I_1^{(i)} + I_2^{(i)} \quad (14)$$

where, $M=48$ is the length of vector $S^{(i)}$;

$S^{(i)} = (S_{(i-1)M+1}, S_{(i-1)M+2}, \dots, S_{(i-1)M+M})^T$ is the signal to be estimated from $e^{(i)}$;

$H^{(i)} = (H^{(i)}_{mn})_{64 \times M}$ is the CIR matrix for i th ($i = 1, \dots, 8$) sub-block, its elements

relates to $h^{(i)}$ vector through the following equation:

$$H^{(i)}_{m,n} = \begin{cases} h^{(i)}_{m-n+1} & \text{for } 1 \leq m-n+1 \leq W \\ 0 & \text{else} \end{cases} \quad (15)$$

$I_1^{(i)} = [\underbrace{0 \dots 0}_{48 \text{ zeros}} \Delta_1^{(i)T}]^T$ of length 64 is the interference caused by unwanted

chips in the same i th ($i = 1, \dots, 8$) sub-blocks ;

$I_2^{(i)} = [\Delta_2^{(i)T} \underbrace{0 \dots 0}_{49 \text{ zeros}}]^T$ of length 64 is the interference caused by chips in the

pervious sub-blocks (note that the first sub-block, i.e. $i = 1$, only suffer from unwanted chips in the same sub-block, therefore $I_2^{(1)} = [\underbrace{0 \ 0 \dots 0}_{64 \text{ zeros}}]^T$)

$\Delta_1^{(i)}$ is the effective error vector with length 16 caused by unwanted chips in the same sub-block, which can be further written as:

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$$\Delta_1^{(i)} = H_1^{(i)}U^{(i)} \quad (16)$$

where, $U^{(i)} = (S_{iM+1}, S_{iM+2}, \dots, S_{iM+16})^T$ of length 16 is the unwanted chips in the i th ($i = 1, \dots, 8$) sub-block other than $S^{(i)}$.

$\Delta_2^{(i)}$ is the effective error vector with length 15 caused by chips from previous ($i -$

1th) ($i = 2, \dots, 8$) sub-block, which can be further written as:

$$\Delta_2^{(i)} = H_2^{(i)}V^{(i)} \quad (17)$$

where, $V^{(i)} = (S_{(i-1)M-14}, S_{(i-1)M-13}, \dots, S_{(i-1)M})^T$ of length 15 is the chips in the previous ($i - 1$ th) ($i = 2, \dots, 8$) sub-blocks.

$H_1^{(i)}$ with dimension of 16×16 can be written as:

$H_1^{(i)}$ with dimension of 16×16 can be written as:

$$H_1^{(i)} = \begin{cases} h^{(i)}_{m-n+1} & \text{for } 1 \leq m-n+1 < 16 \\ 0 & \text{else} \end{cases} \quad (18)$$

$H_2^{(i)}$ with dimension 15×15 , can be written as:

$$H_2^{(i)} = \begin{cases} h^{(i)}_{W-1+m-n} & \text{for } 0 \leq m-n \leq 15 \\ 0 & \text{else} \end{cases} \quad (19)$$

Since $S^{(i)}$ is to be estimated from $e^{(i)}$, it is obvious the observation signal $e^{(i)}$ suffered interference from $U^{(i)}$ and $V^{(i)}$, which, if not subtracted from the $e^{(i)}$, the estimation performance of $S^{(i)}$ will be effected. The illustration of interference with sub-block processing is shown in Figure.6.

In order to improve the estimation performance of $S^{(i)}$, the interference $I_1^{(i)}$ and $I_2^{(i)}$ need to be estimated and subtracted from the $e^{(i)}$. The proposed receiver has two stages (shown in Figure 5): In the first stage, conventional sub-block processing is performed, and data estimation is obtained based on the first sub-block processing. In the second stage, we regenerate the interference caused by adjacent blocks and unwanted chips in the same sub-block and subtract the interference from the received data signal. Then a second sub-block processing is performed to detect data.

20 Stage 1:

1) Calculating vector $g^{(j)}$ of dimension 64 according to (10) and (11):

$$g^{(j)} = IFFT\left(\frac{FFT^*(h^{(j)})FFT(e^{(j)})}{FFT^*(h^{(j)})FFT(h^{(j)}) + \sigma^2}\right) \quad j = 1, \dots, 8$$

where $h^{(j)}$ is the estimation of CIR in the centre of the j th ($j = 1, \dots, 8$) sub-block

2) Estimation of $S^{(j)}$ is obtained by discarding the last 16 items or 48 items of

5 $g^{(j)}$:

$$\hat{S}^{(j)} = \begin{cases} g^{(j)}(1:48) & 1 \leq j \leq 7 \\ g^{(j)}(1:16) & j = 8 \end{cases}$$

Where, $g(m:n)$ denotes taking the element of g with index from m to n .

3) Based on $\hat{S}^{(j)}$ ($j=1, \dots, 8$), the estimation of S can be written as:

$$\hat{S} = [\hat{S}^{(1)T} \quad \hat{S}^{(2)T} \quad \dots \quad \hat{S}^{(8)T}]^T$$

10 4) The continuous-valued estimate of $d(k)$ ($K = 1, \dots, K$) after code matched filtering becomes:

$$\tilde{d}(k) = \frac{1}{Q} C^k H \hat{S}$$

5) A hard decision on $d(k)$ is obtained as:

$$\hat{d}(k) = \text{csign}(\tilde{d}(k))$$

15 where $\text{csign}(x)$ denotes taking the sign bit of the real and imaginary parts of a complex signal x .

Stage 2:

1) Based on the hard decision $\hat{d}(k)$, we can reconstruct superposition of K code channel signal by modulation and spreading, which can be expressed as:

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$$\tilde{S} = (\tilde{S}_1, \tilde{S}_2, \dots, \tilde{S}_{NQ})^T = C \hat{d}$$

where, $\hat{d} = (\hat{d}(1)^T, \hat{d}(2)^T, \dots, \hat{d}(K)^T)^T$ is the combined sequence of all the estimated users data.

2) The effective interference signal $\hat{\Delta}_1^{(j)}$ and $\hat{\Delta}_2^{(j)}$ can be re-generated

25 as $\hat{\Delta}_1^{(j)} = \hat{H}_1^{(j)} \hat{U}^{(j)}$ and $\hat{\Delta}_2^{(j)} = \hat{H}_2^{(j)} \hat{V}^{(j)}$ respectively. Where,

$\hat{U}^{(j)} = (\tilde{S}_{jM+1}, \tilde{S}_{jM+2}, \dots, \tilde{S}_{jM+16})^T$, and $\hat{V}^{(j)} = (\tilde{S}_{(j-1)M-14}, \tilde{S}_{(j-1)M-13}, \dots, \tilde{S}_{(j-1)M})^T$ are respectively the estimation of $U^{(j)}$ and $V^{(j)}$. $\hat{H}_1^{(j)}$ and $\hat{H}_2^{(j)}$ are respectively the estimation of $H_1^{(j)}$ and $H_2^{(j)}$.

3) The interference signal can then be regenerated as

$$\hat{I}_1^{(j)} = [\underbrace{0 \dots 0}_{48 \text{ zeros}} \hat{\Delta}_1^{(j)}]^T \text{ and}$$

$$\hat{I}_2^{(j)} = [\hat{\Delta}_2^{(j)} \underbrace{0 \dots 0}_{49 \text{ zeros}}]^T, \text{ respectively.}$$

4) The regenerated signal is subtracted from received signal $e^{(j)}$:

$$\tilde{e}^{(j)} = e^{(j)} - \hat{I}_1^{(j)} - \hat{I}_2^{(j)} = H^{(j)}S^{(j)} + [I_1^{(j)} - \hat{I}_1^{(j)}] + [I_2^{(j)} - \hat{I}_2^{(j)}] + n(j)$$

Assuming no error in the estimation of $\hat{I}_1^{(j)}$ and $\hat{I}_2^{(j)}$, it can be seen that the interference has been cancelled out from the received signal.

5) For the second time, the vector $\tilde{g}^{(j)}$ of dimension 64 is obtained again as:

$$\tilde{g}^{(j)} = IFFT\left(\frac{FFT^*(h^{(j)})FFT(\tilde{e}^{(j)})}{FFT^*(h^{(j)})FFT(h^{(j)}) + \sigma^2}\right)$$

6) Estimation of $S^{(j)}$ is obtained by discarding the last 16 items or 48 items of $\tilde{g}^{(j)}$:

$$\hat{S}^{(j)} = \begin{cases} \tilde{g}^{(j)}(1:48) & 1 \leq j \leq 7 \\ \tilde{g}^{(j)}(1:16) & j = 8 \end{cases}$$

7) Based on $\hat{S}^{(j)}$ ($j=1, \dots, 8$), the estimation of S can be written as:

$$\hat{S} = [\hat{S}^{(1)T} \quad \hat{S}^{(2)T} \quad \dots \quad \hat{S}^{(8)T}]^T$$

8) The continuous-valued estimate of $d(k)$ after code matched filtering becomes:

$$\tilde{d}(k) = \frac{1}{Q} C^k H \hat{S}$$

9) A final decision on $d(k)$ is obtained as:

$$\hat{d}(k) = csign(\tilde{d}(k))$$

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The performance of the novel sub-block processing of the method of the invention as described above was analyzed by simulation for transmission over mobile radio channels. The transmitted signal is constructed according to LCR TDD-CDMA specification (refer: Ts 25. 221 [1] and Ts 25.223 [2]). The transmitted signal consists of 10 codes, with equal power for each code. Other parameter settings used for the simulation are:

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1) The transmitted data sequence of each of K users in one time slot consists of 44 symbols or 704 chips, and each data part (data part 1 and data part 2) contains $N = 22$ symbols or 352 chips;

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2) The spreading factor, $Q = 16$, i.e., the number of chips per data symbol is 16;

3) The additive noise n is white Gaussian noise with zero mean and covariance matrix $R_n = I$;

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4) Two kinds of mobile radio channel are used: channel A and channel B. Channel A is 3 path rayleigh fading channel, with relative power (0dB, 0dB, 0dB) and relative delay (0, 5chips, 10chips), respectively. Channel B is 4 path rayleigh fading channel, with relative power (0dB, -3dB, -6dB, -9dB) and relative delay (0, 1 chip, 2 chips, 3 chips), respectively. Two kinds of moving speed are simulated: 120km and 250km. The Doppler spread is 222 Hz for 120 km/hr and 462 Hz for 250km/hr.

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5) The number of samples, W , of the channel impulse response at chip interval is 16;

- 6) For both conventional and novel sub-block processing, FFT length of 64 and overlap length of 16 is used.
- 7) For each data part, the channel impulse response in the centre of each sub-block is used for each sub-block and is ideal known to the receiver.

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A BER comparison between conventional sub-block processing and novel sub-block processing according to the invention is shown in Fig.7 and Fig.8 for channel A with a movement speed of 120 km/hr and 250km/hr, respectively. A BER comparison between conventional sub-block processing and novel sub-block processing according to the invention is shown in Fig.9 and Fig.10 for channel B with moving speed 120 km/hr and 250km/hr, respectively. It can be shown that conventional sub-block processing has a BER floor caused by the sub-block interference. The novel sub-block processing of the invention by eliminating the sub-block interference is thus demonstrated to improve performance particularly in a high SNR zone. This is because in the high SNR zone, the first sub-block processing can provide accurate bit estimation, and using this accurate bit estimation, the interference can be regenerated with better accuracy than that can be obtained in low SNR zone. Thus, the interference can be cancelled more effectively and good performance can be obtained. In comparison, the performance of whole block processing using 512 FFT has also been shown. As expected, the whole block processing using 512 FFT has the degraded performance due to no channel tracking and the higher the moving speed, the worse the performance degradation.

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CLAIMS

1. A method of interference reduction in a TD-SCMDA downlink receiver, the method comprising partitioning a received signal into a number of sub-blocks of
5 length N_T with an overlap length N_Z between adjacent sub-blocks and processing said sub-blocks so that substantially only $M = N_T - N_Z$ is extracted as the desired data signal.

2. The method of claim 1, wherein the sub-block processing comprises:

10 (a) applying a first processing operation to the sub-blocks so that the extracted data signal $M = N_T - N_Z$;

15 (b) for each sub-block of the received data signal, regenerating interference caused by adjacent blocks and unwanted chips in the same sub-block;

(c) subtracting the regenerated interference from said received data signal to generate a reduced interference data signal; and

20 (d) applying a second sub-block processing operation to said reduce interference data signal.

3. The method of claim 1, wherein only a feedback component of some detected data symbols is used for cancellation of their associated interference.

25 4. The method of claim 1, wherein an equalizer is applied to detected data symbols and only some of the detected data symbols are used to regenerate the interference.

5. A TD-SCMDA downlink receiver comprising as interference reduction means, means for partitioning a received signal into a number of sub-blocks of length N_T with an overlap length N_Z between adjacent sub-blocks and means for processing said sub-blocks so that substantially only $M = N_T - N_Z$ is extracted as the desired data signal.

6. The receiver of claim 5, wherein said sub-block processing means comprises:

(a) means for applying a first sub-block processing operation to a received data signal;

(b) means for each sub-block of the received data signal, regenerating interference caused by adjacent blocks and unwanted chips in the same sub-block;

(c) means for subtracting the regenerated interference from said received data signal to generate a reduced interference data signal; and

(d) means for applying a second sub-block processing operation to said reduce interference data signal.

7. The receiver of claim 5, wherein only a feedback component of some detected data symbols is used for cancellation of their associated interference.

8. The receiver of claim 5, wherein an equalizer is applied to detected data symbols and only some of the detected data symbols are used to regenerate the interference.