# TIMING CALIBRATION METHOD AND TIMING CALIBRATION SYSTEM

## CROSS REFERENCE TO RELATED APPLICATIONS

This application is a National Phase of International Patent Application No. PCT/CN2022/127520, filed on October 26, 2022, which claims priority to Chinese Patent Application No. 202210115782.8, filed with CNIPA on February 07, 2022, the entire contents of which are incorporated herein in their entireties.

## TECHNICAL FIELD

**[0001]** The present disclosure relates to the field of chip testing, and in particular, to a timing calibration method and a timing calibration system.

## BACKGROUND

**[0002]** A digital chip tester generally supports pattern (test vector) testing, and the pattern testing may be performed to determine whether functions of digital chips are normal, thereby achieving rapid testing of the digital chips during mass production.

**[0003]** The digital chip tester generally supports hundreds of test channels. Digital signals output by respective test channels are required to be simultaneously output to pins of a digital chip under test. That is, the digital signals are required to be edge-aligned to ensure that timing among the signals output to the pins of the digital chip under test is correct. To ensure edge alignment of digital signals output by all test channels of all digital chip testers, there is a need to perform timing calibration on the digital signals.

**[0004]** In an existing method, a high-speed oscilloscope is generally used to determine whether test edges of the test channels are aligned one by one. This method requires an additional high-speed oscilloscope, which is expensive and inconvenient to use. Alternatively, clock signals output by two channels are ANDed, and then it is determined whether the clock signals are edge-aligned by performing capacitor charging and then voltage collection using the ANDed signal. The method requires capacitor charging and analog-to-digital converter (ADC) sampling, resulting in long test time.

## SUMMARY

**[0005]** One objective of the present disclosure is to provide a timing calibration method and a timing calibration system to solve at least one of the problems existing in the prior art.

**[0006]** To achieve the above objective, the present disclosure adopts the following technical solutions.

**[0007]** In a first aspect of the present disclosure, a timing calibration method is provided, applied for performing timing calibration on test signals in a number of test channels of a digital tester, the method including:

**[0008]** gating any two test channels of the digital tester to output test signals;

**[0009]** comparing, by using a window comparator, the test signals output by the two gated test channels, and outputting a comparison result to a field-programmable gate array (FPGA);

**[0010]** transmitting, via a clock buffer, the test signal output by one of the two gated test channels to the FPGA, the test signal serving as a sampling clock;

**[0011]** collecting, by the FPGA according to the sampling clock, the comparison result output by the window comparator, and sending the comparison result to a control terminal; and

**[0012]** adjusting, by the control terminal, a clock phase of the test signal in a corresponding test channel according to the comparison result output by the FPGA, to complete timing calibration of the test channel.

**[0013]** Optionally, the method further includes: taking the test channel where the sampling clock is from as a calibration reference channel, and sequentially gating one of the other test channels to be in communication with the window comparator to serve as a calibrated channel for timing calibration.

**[0014]** Optionally, multiple excitation signal test channels of the digital tester are connected to an input end of a relay network, a first output end of the relay network is connected to a first input end of the window comparator, a second output end of the relay network is connected to a second input end and of the window comparator and an input end of the clock buffer, an output end of the window comparator is connected to a first input end of the FPGA, an output end of the clock buffer is connected to a second input end of the FPGA, and an output end of the FPGA is connected to the control terminal.

**[0015]** Optionally, the control terminal controls relays in the relay network to be turned

on or turned off, to output two gated excitation signal test channels to the first output end and the second output end of the relay network respectively.

**[0016]** Optionally, if an edge of a clock signal generated by the calibrated channel is not aligned with an edge of a clock signal generated by the reference channel, the control terminal controls the excitation signal test channel of the digital tester to adjust the clock phase output by the calibrated channel until the clock phase of the calibrated channel is aligned with the edge of the clock signal generated by the reference channel.

**[0017]** Optionally, the clock phase output by the calibrated channel is adjusted by binary search.

**[0018]** Optionally, if it is detected that a phase of the calibrated channel is in advance of that of the reference channel, an output delay of the calibrated channel is set to be N nS, if it is detected in this case that the phase of the calibrated channel lags behind that of the reference channel, the output delay of the calibrated channel is adjusted to be N/2 nS; if it is detected in this case that the phase of the calibrated channel lags behind that of the reference channel, the phase of the calibrated channel is in advance of that of the reference channel within a range from 0 nS to N/2 nS, and if it is detected in this case that the phase of the calibrated channel is in advance of that of the reference channel, the phase of the calibrated channel is in advance of that of the reference channel within a range from N/2 nS to N nS, where N>0.

**[0019]** In a second aspect of the present disclosure, a timing calibration system for performing the above timing calibration method is provided, where the system includes: a digital tester, a control terminal, and a timing calibration board;

**[0020]** the timing calibration board includes: a relay network, a window comparator, a clock buffer, and an FPGA; where

**[0021]** the digital tester includes multiple excitation signal test channels;

**[0022]** the relay network is configured to gate any two of the multiple excitation signal test channels of the digital tester and output the two excitation signal test channels to the window comparator respectively;

**[0023]** the window comparator is configured to compare clock signals output by the two gated excitation signal test channels, determine whether edges of the two clock signals are aligned, and output a comparison result to the FPGA;

**[0024]** the clock buffer is configured to buffer the clock signal output by one of the gated excitation signal test channels and then output the clock signal to the FPGA as a

sampling clock;

**[0025]** the FPGA is configured to collect the comparison result of the window comparator according to the sampling clock, and send the comparison result to the control terminal; and

**[0026]** the control terminal is configured to control the excitation signal test channels to generate clock signals, determine whether the clock signals generated by two excitation signal test channels are edge-aligned, and perform timing calibration.

**[0027]** Optionally, the relay network and the window comparator support operating frequencies ranging from 100 MHz to 800 MHz.

**[0028]** Optionally, the control terminal controls the relay network to gate one of the test channels to be in communication with an input end of the clock buffer and a second input end of the high-speed window comparator to serve as a calibration reference channel, and sequentially gates one of the other excitation signal test channels to be in communication with a first input end of the window comparator to serve as a calibrated channel for timing calibration.

**[0029]** The present disclosure has the following beneficial effects.

**[0030]** According to the technical solutions of the present disclosure, a timing calibration method and a timing calibration system are provided. The system can achieve timing calibration without any external instrument such as an oscilloscope, so it is easy to use. According to the timing calibration method of the present disclosure, by use of a high-speed relay network and a high-speed window comparator in a timing calibration board, timing calibration of test channels of a digital tester can be quickly realized, improving timing calibration efficiency. Moreover, calibration accuracy of all test channels can be ensured within 50 ps, meeting a calibration accuracy requirement.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0031]** Specific implementations of the present disclosure are described in further detail below with reference to accompanying drawings.

**[0032]** FIG. 1 is a schematic diagram of a timing calibration system according to an embodiment of the present disclosure; and

**[0033]** FIG. 2 is a flowchart of a timing calibration method according to an embodiment of the present disclosure.

## DETAILED DESCRIPTION OF THE EMBODIMENTS

**[0034]** In order to illustrate the present disclosure more clearly, the present disclosure is further described below according to preferred embodiments in conjunction with the accompanying drawings. Similar parts are represented by an identical reference numeral in the drawings. Those skilled in the art should understand that the content specified below is illustrative rather than restrictive, and should not be used to limit the protection scope of the present disclosure.

**[0035]** As shown in FIG. 1, a timing calibration system is provided according to an embodiment of the present disclosure, including a digital tester 1, a control terminal 2, and a timing calibration board 3.

**[0036]** The digital tester 1 includes a number of test channels. One test vector (pattern) is correspondingly transmitted in each test channel. The test vector is sent as a test signal by the digital tester to a pin of a product under test. Commonly, the digital tester 1 may include 512, 768, or 1024 test channels. That is, 512 test vectors are correspondingly transmitted in 512 test channels.

**[0037]** The control terminal 2 may be a computer or a cloud server, and is mainly configured to control conduct of a timing calibration process.

**[0038]** The timing calibration board 3 includes: a high-speed relay network 31, a high-speed window comparator 32, a clock buffer 33, and an FPGA 34.

**[0039]** The high-speed relay network 31 is configured to gate any two test channels of the digital tester, so that two test vectors in the two gated test channels are output to the high-speed window comparator 32 respectively. In a specific example, the high-speed relay network 31 and the high-speed window comparator 32 support a maximum operating frequency of 800 MHz.

**[0040]** The high-speed window comparator 32 is configured to compare test vector signals output by the two gated test channels, determine whether edges of the two test vector signals are aligned, and output a comparison result to the FPGA 34.

**[0041]** The clock buffer 33 is configured to buffer the test vector signal generated by one of the gated test channels and then output the buffered test vector signal to the FPGA 34 as a sampling clock.

**[0042]** The FPGA 34 is configured to collect, according to the sampling clock, the comparison result of the high-speed window comparator 32, and send the comparison result

to the control terminal 2.

**[0043]** The control terminal 2 is configured to control excitation signal test channels to generate clock signals, determine whether the clock signals generated by two excitation signal test channels are edge-aligned, and perform timing calibration.

**[0044]** In a possible implementation, the relay network and the window comparator support operating frequencies ranging from 100 MHz to 800 MHz.

**[0045]** In a possible implementation, the control terminal controls the relay network to gate one of the test channels to be in communication with an input end of the clock buffer and a second input end of the window comparator to serve as a calibration reference channel, and sequentially gate one of the other excitation signal test channels to be in communication with a first input end of the high-speed window comparator to serve as a calibrated channel for timing calibration.

**[0046]** As shown in FIG. 2, a timing calibration method is provided according to another embodiment of the present disclosure, used for performing timing calibration on test signals in a number of test channels of a digital tester. The method includes:

gating any two test channels of the digital tester to output test signals;

comparing, by using a window comparator, the test signals output by the two gated test channels, and outputting a comparison result to an FPGA;

transmitting, via a clock buffer, the test signal output by one of the two gated test channels to the FPGA, the test signal serving as a sampling clock;

collecting, by the FPGA according to the sampling clock, the comparison result output by the window comparator, and sending the comparison result to a control terminal; and

adjusting, by the control terminal, a clock phase of the test signal in a corresponding test channel according to the comparison result output by the FPGA, to complete timing calibration of the test channel.

**[0047]** In a possible implementation, multiple excitation signal test channels of the digital tester 1 are connected to an input end of the high-speed relay network 31, a first output end of the high-speed relay network 31 is connected to a first input end of the high-speed window comparator 32, a second output end of the high-speed relay network 31 is connected to a second input end and of the high-speed window comparator 32 and an input end of the clock buffer 33, an output end of the high-speed window comparator 32 is connected to a first input end of the FPGA 34, an output end of the clock buffer 33 is

connected to a second input end of the FPGA 34, and an output end of the FPGA 34 is connected to the control terminal 2.

**[0048]** In a possible implementation, the control terminal 2 controls relays in the high-speed relay network 31 to be turned on or turned off, to output two gated excitation signal test channels to the first output end and the second output end of the high-speed relay network 31 respectively.

**[0049]** In a specific example, at least 512 test channels included in the digital tester 1 are all connected to the input end of the high-speed relay network 31, the 512 test channels correspondingly transmit 512 test vectors (patterns), the high-speed relay network 31 arbitrarily selects two test channels from the at least 512 test channels included in the digital tester 1 for output; two output ends of the high-speed relay network 31 are both connected to input ends of the high-speed window comparator 32, at the same time, one of the output ends of the high-speed relay network 31 is connected to the input end of the clock buffer 33, the output end of the high-speed window comparator 32 is connected to the FPGA, the output end of the clock buffer 33 is connected to the FPGA, and the FPGA uses the sampling clock output by the clock buffer 33 to sample the comparison result of the high-speed window comparator 32, and then transmits a sampling result to the control terminal 2. For example, the control terminal 2 is a computer, and the computer determines whether the two test channels in a current test are edge-aligned and performs timing calibration.

**[0050]** In a possible implementation, the control terminal 2 controls the high-speed relay network 31 to: gate one of the test channels to be in communication with the input end of the clock buffer 33 and the second input end of the high-speed window comparator 32 to serve as a calibration reference channel, the reference channel being referred to as Channel 2, and sequentially gate one of the other excitation signal test channels to be in communication with the first input end of the high-speed window comparator to serve as a calibrated channel for timing calibration, the calibrated channel being referred to as Channel 1.

**[0051]** In a specific example, the control terminal 2 sequentially gates other excitation signal test channels that have not been gated by the high-speed window comparator 32, and performs timing calibration on the calibrated channel 1 according to the reference channel 2.

**[0052]** In a specific example, the computer controls the two gated excitation signal test

channels in the digital tester to generate clock signals. For example, the clock signals are clock signals of 100 MHz.

**[0053]** In a possible implementation, the method further includes: taking the test channel where the sampling clock is from as a calibration reference channel, and sequentially gating one of the other test channels to be in communication with the window comparator to serve as a calibrated channel for timing calibration.

**[0054]** In a possible implementation, if an edge of a clock signal generated by the calibrated channel is not aligned with an edge of a clock signal generated by the reference channel, the control terminal controls the excitation signal test channels of the digital tester to adjust a clock phase output by the calibrated channel until the clock phase of the calibrated channel is aligned with the edge of the clock signal generated by the reference channel.

**[0055]** In a specific example, in a case that the comparison result output by the high-speed window comparator is random 0 and 1, the clock signals generated by the calibrated channel and the reference channel are edge-aligned; in a case that the comparison result output by the high-speed window comparator is fixed 0 or 1, the clock signals generated by the calibrated channel and the reference channel are not edge-aligned. Accordingly, whether the clock signals generated by the calibrated channel and the reference channel are edge-aligned can be determined, thereby achieving timing calibration.

**[0056]** In a case that the clock signals generated by the calibrated channel and the reference channel are not edge-aligned, the control terminal 2 controls the digital tester 1 to adjust a clock phase output by the calibrated channel until the clock signals generated by the calibrated channel and the reference channel are edge-aligned. The clock phase output by the calibrated channel is adjusted by binary search so that the clock signals generated by the calibrated channel and the reference channel are edge-aligned.

**[0057]** In a possible implementation, if it is detected that a phase of the calibrated channel is in advance of that of the reference channel, an output delay of the calibrated channel is set to be N nS, then if it is detected in this case that the phase of the calibrated channel lags behind that of the reference channel, the output delay of the calibrated channel is adjusted to be N/2 nS; furthermore, if it is detected in this case that the phase of the calibrated channel lags behind that of the reference channel, the phase of the calibrated channel shall be in advance of that of the reference channel within a range from 0 nS to N/2 nS, and if it is detected in this case that the phase of the calibrated channel is in advance of

that of the reference channel, the phase of the calibrated channel shall be in advance of that of the reference channel within a range from N/2 nS to N nS, where N>0.

**[0058]** In a specific example, Channel 1 is the calibrated channel, that is, the one of the other excitation signal test channels in communication with the first input end of the high-speed window comparator; Channel 2 is the reference channel, that is, the one of the two gated excitation signal test channels communicated by the high-speed relay network with the input end of the clock buffer and the second input end of the high-speed window comparator. When none of Channel 1 and Channel 2 has an output delay, it is detected that a phase of Channel 1 is in advance of that of Channel 2, and the output delay of Channel 1 is increased by 5 nS. Then, if it is detected that the phase of Channel 1 lags behind that of Channel 2, the output delay of Channel 1 is modified to 2.5 nS. Then, if it is detected that the phase of Channel 1 lags behind that of Channel 2, the phase of Channel 1 shall be in advance of that of Channel 2 within a range from 0 nS to 2.5 nS; if it is detected that the phase of Channel 1 is in advance of that of Channel 2, the phase of Channel 1 shall be in advance of that of Channel 2 within a range from 2.5 nS to 5 nS. By means of determination based on the range and further sequentially performed binary searches and determinations, an actual phase difference is finally found.

**[0059]** The calibration of the timing calibration system provided in the present disclosure does not require the connection of the digital chip under test. After the calibration is completed, the digital tester is connected to the digital chip under test.

**[0060]** In a specific example, calibration accuracy of the reference channel and all the calibrated channels of the timing calibration system of the present disclosure is 50 ps, and the accuracy is mainly related to parameters of the high-speed window comparator.

**[0061]** It is to be noted that the principle and workflow of the timing calibration system provided in the embodiment are similar to those of the above timing calibration method. Related content may be obtained with reference to the above description, which will not be repeated herein.

**[0062]** According to the timing calibration system and the timing calibration method provided in the embodiments of the present disclosure, there is no need to connect an external instrument such as an oscilloscope, and the high-speed window comparator is used, which can quickly realize timing calibration of pattern test channels of the digital tester, improving timing calibration efficiency. Moreover, calibration accuracy can be ensured within 50 ps, meeting a calibration accuracy requirement.

**[0063]** Obviously, the above embodiments of the present disclosure are only examples to clearly illustrate the present disclosure, and are not intended to limit the implementations of the present disclosure. For those of ordinary skill in the art, other different forms of changes or modifications may also be made based on the above description, and it is impossible to exhaustively list all the implementations herein. Any obvious change or modification derived from the technical solutions of the present disclosure still falls within the protection scope of the present disclosure.

## CLAIMS

1. A timing calibration method, which is applied for performing timing calibration on test signals in a number of test channels of a digital tester, comprising:

gating any two test channels of the digital tester to output test signals;

comparing, by using a window comparator, the test signals output by the two gated test channels, and outputting a comparison result to a field-programmable gate array (FPGA);

transmitting, via a clock buffer, the test signal output by one of the two gated test channels to the FPGA, the test signal serving as a sampling clock;

collecting, by the FPGA according to the sampling clock, the comparison result output by the window comparator, and sending the comparison result to a control terminal; and

adjusting, by the control terminal, a clock phase of the test signal in a corresponding test channel according to the comparison result output by the FPGA, to complete timing calibration of the test channel.

2. The timing calibration method according to claim 1, further comprising: taking the test channel where the sampling clock is from as a calibration reference channel, and sequentially gating one of the other test channels to be in communication with the window comparator to serve as a calibrated channel for timing calibration.

3. The timing calibration method according to claim 1, wherein a plurality of excitation signal test channels of the digital tester are connected to an input end of a relay network, a first output end of the relay network is connected to a first input end of the window comparator, a second output end of the relay network is connected to a second input end of the window comparator and an input end of the clock buffer, an output end of the window comparator is connected to a first input end of the FPGA, an output end of the clock buffer is connected to a second input end of the FPGA, and an output end of the FPGA is connected to the control terminal.

4. The timing calibration method according to claim 3, wherein the control terminal controls relays in the relay network to be turned on or turned off, to output two gated excitation signal test channels to the first output end and the second output end of the relay network respectively.

5. The timing calibration method according to claim 2, wherein if an edge of a clock signal generated by the calibrated channel is not aligned with an edge of a clock signal generated by the reference channel, the control terminal controls excitation signal test channels of the digital tester to adjust the clock phase output by the calibrated channel until the clock phase of the calibrated channel is aligned with the edge of the clock signal generated by the reference channel.

6. The timing calibration method according to claim 5, wherein the clock phase output by the calibrated channel is adjusted by binary search.

7. The timing calibration method according to claim 6, wherein if it is detected that a phase of the calibrated channel is in advance of that of the reference channel, an output delay of the calibrated channel is set to be N nS, then if it is detected in this case that the phase of the calibrated channel lags behind that of the reference channel, the output delay of the calibrated channel is adjusted to be N/2 nS; if it is detected in this case that the phase of the calibrated channel lags behind that of the reference channel, the phase of the calibrated channel is in advance of that of the reference channel within a range from 0 nS to N/2 nS, and if it is detected in this case that the phase of the calibrated channel is in advance of that of the reference channel, the phase of the calibrated channel is in advance of that of the reference channel within a range from N/2 nS to N nS, where N>0.

8. A timing calibration system, which is for performing the timing calibration method according to any one of claims 1 to 7, wherein the timing calibration system comprises: a digital tester, a control terminal, and a timing calibration board, and the timing calibration board comprises: a relay network, a window comparator, a clock buffer, and an FPGA; wherein

the digital tester comprises a plurality of excitation signal test channels;

the relay network is configured to gate any two of the plurality of excitation signal test channels of the digital tester and output the two excitation signal test channels to the window comparator respectively;

the window comparator is configured to compare clock signals output by the two gated excitation signal test channels, determine whether edges of the two clock signals are aligned, and output a comparison result to the FPGA;

the clock buffer is configured to buffer the clock signal output by one of the gated excitation signal test channels and then output the clock signal to the FPGA as a sampling clock;

the FPGA is configured to collect the comparison result of the window comparator according to the sampling clock, and send the comparison result to the control terminal; and

the control terminal is configured to control the excitation signal test channels to generate clock signals, determine whether the clock signals generated by two excitation signal test channels are edge-aligned, and perform timing calibration.

9. The timing calibration system according to claim 8, wherein the relay network and the window comparator support operating frequencies ranging from 100 MHz to 800 MHz.

10. The timing calibration system according to claim 8, wherein the control terminal controls the relay network to: gate one of the test channels to be in communication with an input end of the clock buffer and a second input end of the window comparator to serve as a calibration reference channel, and sequentially gate one of the other excitation signal test channels to be in communication with a first input end of the window comparator to serve as a calibrated channel for timing calibration.