WHAT IS CLAIMED IS:

1. A capacitor, comprising:

a lower electrode;

a dielectric layer structure on the lower electrode, the dielectric layer structure including a first zirconium oxide layer, a hafnium oxide layer, and a second zirconium oxide layer sequentially stacked; and

an upper electrode on the dielectric layer structure,

wherein the hafnium oxide layer has a tetragonal crystal phase or an orthorhombic crystal phase, and

wherein the dielectric layer structure further includes an interface layer, the interface layer being between the first zirconium oxide layer and the lower electrode.

2. The capacitor as claimed in claim 1, wherein the first zirconium oxide layer and the second zirconium oxide layer are each crystalline.

3. The capacitor as claimed in claim 2, wherein the first zirconium oxide layer and the second zirconium oxide layer have an orthorhombic crystal phase.

4. The capacitor as claimed in any one of claims 1 to 3, wherein the hafnium oxide layer has a thickness of 5 Å to 18 Å.

5. The capacitor as claimed in any one of claims 1 to 4, wherein each of the first zirconium oxide layer and the second zirconium oxide layer independently has a thickness of 5 Å to 30 Å.

6. The capacitor as claimed in any one of claims 1 to 5, wherein the dielectric layer structure has a thickness of 20 Å to 60 Å.

7. The capacitor as claimed in claim 6, wherein the interface layer includes a ZrNbOx layer, a TiNbOx layer, or a stacked structure of the TiNbOx layer and the ZrNbOx layer.

8. The capacitor as claimed in any one of claims 1 to 7, wherein the dielectric layer structure further includes an insert layer and a third zirconium oxide layer, the insert layer including an oxide of Al, Ta, Nb, Mo, W, Ru, V, Y, Sc, or Gd.

9. The capacitor as claimed in claim 8, wherein the insert layer and the third zirconium oxide layer are amorphous.

10. The capacitor as claimed in any one of claims 1 to 9, wherein the lower electrode includes a metal, a metal nitride, or a conductive oxide.

11. A capacitor, comprising:

a lower electrode;

a dielectric layer structure on the lower electrode, the dielectric layer structure including a first zirconium oxide layer, a hafnium oxide layer, and a second zirconium oxide layer sequentially stacked; and

an upper electrode on the dielectric layer structure,

wherein:

the dielectric layer structure has a thickness of 20 Å to 60 Å, and

the first zirconium oxide layer, the hafnium oxide layer, and the second zirconium oxide layer are each crystalline,

wherein the dielectric layer structure further includes an interface layer, the interface layer being between the first zirconium oxide layer and the lower electrode.

12. The capacitor as claimed in claim 11, wherein the hafnium oxide layer has a tetragonal crystal phase or an orthorhombic crystal phase.

13. The capacitor as claimed in claim 11 or claim 12, wherein the first zirconium oxide layer and the second zirconium oxide layer each have a tetragonal crystal phase.

14. The capacitor as claimed in any one of claims 11 to 13, wherein the hafnium oxide layer has a thickness of 5 Å to 18 Å.

15. The capacitor as claimed in any one of claims 11 to 14, wherein each of the first zirconium oxide layer and the second zirconium oxide layer independently has a thickness of 5 Å to 30 Å.

16. The capacitor as claimed in any one of claims 11 to 15, wherein:

the dielectric layer structure further includes an insert layer and a third zirconium oxide layer, and

the insert layer includes an oxide of Al, Ta, Nb, Mo, W, Ru, V, Y, Sc, or Gd.

17. A dynamic random-access memory (DRAM) device, comprising:

a substrate;

a cell transistor on the substrate, the cell transistor including a gate structure, a first impurity region, and a second impurity region;

a bit line structure electrically connected to the first impurity region; and

a capacitor on the bit line structure, the capacitor being electrically connected to the second impurity region,

wherein the capacitor includes:

a lower electrode;

a dielectric layer structure on the lower electrode, the dielectric layer structure including a first zirconium oxide layer, a hafnium oxide layer, and a second zirconium oxide layer sequentially stacked; and

an upper electrode on the dielectric layer structure,

wherein the dielectric layer structure further includes an interface layer, the interface layer being between the first zirconium oxide layer and the lower electrode,

wherein the dielectric layer structure has a thickness of 20 Å to 60 Å, and

wherein the hafnium oxide layer has a tetragonal crystal phase or an orthorhombic crystal phase.

18. The DRAM device as claimed in claim 17, wherein the first zirconium oxide layer and the second zirconium oxide layer are each crystalline.