METHOD OF FORMING MOS/CMOS DEVICES WITH DUAL OR TRIPLE GATE OXIDE

ABSTRACT

A method of fabricating multiple thickness gate oxide layers, comprising the following steps. A silicon substrate having at least a first and second gate oxide region is provided. A first gate oxide layer is formed over the silicon substrate within the first gate oxide region. The first gate oxide layer having a first predetermined thickness. A first layer of polysilicon is deposited and planarized over the first gate oxide layer. The first planarized layer of polysilicon and the first gate oxide layer are masked and etched within the second gate oxide region, exposing the silicon substrate within the second gate oxide region. A second gate oxide layer is formed over the exposed silicon substrate within the second gate oxide region. The second gate oxide layer having a second predetermined thickness. A second layer of polysilicon is selectively deposited over the second gate oxide layer. The first and second layers of polysilicon are planarized to a uniform thickness. Whereby the second gate oxide layer predetermined thickness is less than the first gate oxide layer predetermined thickness.

Figure 4