The present invention relates to a device for halting the running of programs being executed in a microprocessor prior to the discontinuance of the supply voltage of the microprocessor.

It is known, in the way described for example in the patent application FR A 2,454,137, to apply a control voltage to the input commonly called the $\overline{\text{RESET}}$ input of a microprocessor in order to reinitialise the latter at the time of mains supply failures. It is also known, in the case in which the execution of a saving subroutine is necessary, to apply this control voltage at an instant which is delayed with respect to an instant of detection of the discontinuance of the mains by a time sufficient to allow the execution of a program for saving the instruction which is being executed.

This arrangement, however, has the disadvantage that it does not provide any security with regard to the functioning of the microprocessor when the supply output voltage happens to disappear for a cause other than the discontinuance of the mains voltage, this event being able to occur in particular when there is a short-circuit on the power supply output or in the case of an accidental disconnection of the microprocessor support board from its power supply. In effect, in these cases the microprocessor reinitialisation voltage cannot be applied to the $\overline{\text{RESET}}$ input because the mains voltage is still present and the supply voltage of the microprocessor disappears. This results in an uncertain functioning of the microprocessor which can generate, on its input-output channel, erratic data which can be harmful to the functioning of the reception devices coupled to the microprocessor by this channel.

In the case in which the execution of a saving subroutine is not necessary, the known arrangement has the additional disadvantage of uselessly complicating the power supply of the microprocessor, as it does not appear essential in this case to have a logic signal available prior to the start of the diminishing of the microprocessor supply voltage while it would suffice simply to

apply a logic voltage equal to 0 volts to the $\overline{\text{RESET}}$ input as soon as the microprocessor supply voltage happens to disappear.

The purpose of the invention is to overcome the abovementioned disadvantages.

For this purpose, the subject of the invention is a device for halting the running of programs being executed in a microprocessor provided with an initialising $\overline{\text{RESET}}$ input and with a supply earth prior to the discontinuance of the supply voltage of the microprocessor, of the type comprising a differentiating circuit connected by way of diversion between a supply line VA of the microprocessor and the supply earth of the microprocessor and a current amplifier coupled between the differentiating circuit and the $\overline{\text{RESET}}$ input of the microprocessor, characterised in that it comprises:

- a capacitor connected on the one hand in parallel between the $\overline{\text{RESET}}$ input and the supply earth of the microprocessor and on the other hand in series between the supply line VA of the microprocessor and the supply earth through a resistor in order to initialise the microprocessor at the time the supply voltage decreases,

- and in that the differentiating circuit comprises means in order to control the current amplifier in order to rapidly discharge the capacitor when the supply voltage begins to diminish.

From the document DE-A-2,936,683, it is known to apply a control voltage on the $\overline{\text{RESET}}$ input of a microprocessor in order to reinitialise it when the supply voltage passes through a lower limit, the device comprising a capacitor connected, on the one hand, in parallel between the $\overline{\text{RESET}}$ input and the supply earth of the microprocessor and, on the other hand, in series between the supply line of the microprocessor and the supply earth across a resistor.

The advantage of the device according to the invention is that it allows the application on the $\overline{\text{RESET}}$ terminal of the microprocessor of a logic voltage equal

to 0 volt as soon as the supply voltage begins to diminish. Another of its advantages is that it allows the microprocessor to be made integral with its protection system, it being possible to achieve this in a simple way by placing the microprocessor and the protection system close to each other on the same support board. The support board for the microprocessor and its protection system will consequently, according to this latter configuration, be able to be connected and disconnected at will to or from any source able to supply the supply voltage of the microprocessor even if that source has no system or device for monitoring the supply voltage level.

Other characteristics and advantages of the invention will also appear with the help of the description referring to the appended drawings which are given solely by way of example and in which:

- Figure 1 shows an embodiment of the device according to the invention;

- Figure 2 shows a variant embodiment of the device according to the invention;

- Figure 3 shows an application of the device according to the invention to the production of a device for saving the instructions of programs being executed in a microprocessor at the time of mains voltage supply failures.

The device according to the invention is shown at 1 in Figure 1 inside a box drawn in dotted lines, connected to the dc voltage supply line of a microprocessor 3, of the type of those for example known by the references 8048/8049 marketed by the SIGNETICS company. The device 1 comprises a differentiating circuit 4 and a current amplifier 5 also shown inside dotted lines. The differentiating circuit 4 is constituted by a resistor 6 and a capacitor 7 connected in series between the dc current and voltage output terminals 8 and 9 of the power supply 2 and a transistor 10. The current amplifier 5 comprises a transistor 11. The transistor 10 is of the NPN type and it is connected by its base on the one hand to the terminal 9 of the power supply 2 and, on

the other hand, to an end of a resistor 6 which is not common with the end of the capacitor 7, via an earth line M of the device. The transistor 11 is of the PNP type and is connected by its base to the collector of the transistor 10 and by its collector to the earth line M of the device. The emitter of the transistor 11 is connected, on the one hand, to the $\overline{\text{RESET}}$ input of the microprocessor 3 and, on the other hand, to the terminal 8 of the power supply 2 via a resistor 12 which in the case of 8048/8049 microprocessors is integrated in the microprocessor. A capacitor 13 is connected in parallel between the emitter of the transistor 11 and the earth line M of the device, and a diode 14 is connected in parallel between the ends of the resistor 6, the anode of the diode 14 being connected to the point common to the resistor 6 and to the capacitor 7, the cathode of the diode 14 being connected to the earth line M of the device.

The functioning of the device which has just been described is as follows. At the moment of switching on, the initialisation of the microprocessor 3 is carried out by means of the capacitor 13 which charges up through the resistor 12 to the dc potential level VA supplied on the terminal 8 of the power supply 2, the capacitor 7 also charges up to the potential level VA through the diode 14 and then the resistor 6. In stabilised conditions, when the potential VA supplied by the stabilised power supply maintains an almost constant value, the $\overline{\text{RESET}}$ input of the microprocessor is taken to the potential level VA and the point common to the capacitor 7 and to the resistor 6 is taken to the potential of the earth line M of the device. When, for any reason whatsoever, the potential VA begins to diminish, the instantaneous variations of the potential VA are transmitted through the capacitor 7 to the point common to the resistor 6 and to the capacitor 7 in such a way that the potential at this common point is taken to a level which is negative with respect to the earth line M, which causes the appearance of a current in the collector-emitter space of the transistor 10, this current being amplified by the transistor 11 which very

rapidly discharges the capacitor 13 into its collector-emitter space and puts the $\overline{\text{RESET}}$ input of the microprocessor 3 at the potential of the earth line M. The setting of the $\overline{\text{RESET}}$ input to the earth potential causes the zero resetting of the program counter of the microprocessor 3 and the reinitialisation of the internal circuits of the microprocessor by interrupting the program which is being executed.

In order to obtain an optimum functioning of the device which has just been described, it is necessary to give the capacitors 7 and 13 and the transistor 11 characteristics such that it is possible to obtain a diminishing of the voltage applied to the $\overline{\text{RESET}}$ terminal of the microprocessor 3 which is much faster than the diminishing of the potential VA supplied by the stabilised power supply 2. If VB denotes the potential which is applied by the emitter of the transistor 11 to the $\overline{\text{RESET}}$ input of the microprocessor 3, the condition which has just been described is written

$$\left|\frac{dVB}{dT}\right| \gg \left|\frac{dVA}{dT}\right| \quad (1).$$

If C_3 denotes the capacity of the capacitor 13, β denotes the current gain of the transistor 11 and C_2 denotes the capacity of the capacitor 7, the expression for the current I passing through the capacitor 13 can be put in the form:

$$I = C_3 \frac{dVB}{dT} = \beta \times C_2 \frac{dVA}{dT}$$

which implies the expression

$$\frac{dVB}{dt} / \frac{dVA}{dt} = \frac{\beta . C_2}{C_3} .$$

The expression (1) therefore appears verified if the values of β, C_2 and C_3 are related by the expression

$$\frac{\beta . C_2}{C_3} \gg 1 .$$

In practice it suffices to choose values for β, C_2 and C_3 such that the expression $\frac{\beta \cdot C_2}{C_3} \geqslant 10$

is satisfied. For example, the abovementioned conditions can be verified by choosing a value of 1 microfarad for C_3, a value which is larger than or equal to 100 β for and a value which is larger than or equal to 0.1 microfarad for C_2.

In the example which has just been described the resistor 6 ensures the charging of the capacitor 7 between a voltage VA - 0.6 volts and the nominal voltage VA of the power supply, the 0.6 volts corresponding to the threshold of the diode 14 if it is a silicon diode.

Under these conditions, the acceptable variation of the potential VA supplied by the power supply 2 without there being any initialisation of the microprocessor 3 is equal to the base-emitter junction threshold of the transistor 10, that is to say 0.6 V if the transistor 10 is a silicon transistor. If the resistor 6 is omitted, the acceptable variation of the potential VA is theoretically equal to the sum of the threshold voltages of the diode 14 and of the base-emitter junction of the transistor 10 (1.2 V if the diode 14 and the transistor 10 are both made of silicon) but in practice the leakage resistances of the diode 14, of the base-emitter junction of the transistor 10 and of the capacitor 7, when combined, will take the acceptable variation of VA to a value included between the threshold voltage of the base-emitter junction of the transistor 10 and of the diode 14. This value being limited but indeterminate, it is advised, if it is desired to obtained an acceptable variation of VA which is greater than the threshold voltage of the base-emitter junction of the transistor 10, not to remove the resistor 6 but to add, between the emitter of the transistor 10 and the point common to the capacitor 7 and to the resistor 6, one or more diodes in series (with the anode on the side of the emitter of the transistor 10). The acceptable variations in the

potential of VA are then equal to the sum of the threshold voltages of the added diodes and of the base-emitter junction of the transistor 10.

The invention is not limited to the embodiment which has just been described and it is quite obvious that other embodiments are still possible without thereby departing from the scope and extent of the invention. In particular, a device according to the invention equivalent to that which has just been described could be obtained by means of transistors 10 and 11 which are complementary to those used for producing the device of Figure 1, the corresponding layout being shown in Figure 2. In this case, the collector of the transistor 11 must be connected to the $\overline{\text{RESET}}$ input of the microprocessor 3 and the order of connecting the resistor 6 and the capacitor 7 to the terminals 8 and 9 of the power supply 2 must be changed around. In this case also, the anode of the diode 14 must be connected to the terminal 8 of the power supply 2, its cathode remaining connected to the point common to the resistor 6 and to the capacitor 7 in order to allow the charging of the capacitor 7 through the diode 14.

According to yet another embodiment of the invention, an even faster response of the device could be obtained by replacing, for example, the transistor 11 by two transistors coupled together to form an amplifier of the type known by the name DARLINGTON in order to obtain a very high current gain.

A use of the device according to the invention for saving programs being executed in a microprocessor when a mains failure appears is now described with reference to the application block diagram shown in Figure 3. In Figure 3, the power supply 2 is connected to the mains by means of a primary winding 15 of a transformer 16 coupled to the power supply 2 by a secondary winding 17. The power supply 2 comprises, in a known way, a rectifier bridge 18 supplied by the secondary winding 17 and a regulator 19 supplied by the outputs of the rectifier bridge 18. The transformer 16 has a second

secondary winding 20 which supplies a mains current absence detector 21, the function of the detector 21 being to apply a constant voltage VL to the interrupt input INT of the microprocessor 3. As explained before, the output of the device 1 of the invention is connected to the $\overline{\text{RESET}}$ input of the microprocessor 3. When a mains voltage supply failure occurs, this failure is detected by the mains voltage absence detector 21 which reacts by applying a zero voltage level to the INT input of the microprocessor 3, which interrupts the program being executed and initiates the saving subroutine. As the regulator 19 comprises, in a way which is known but not shown, a filtering stage placed upstream of the regulation, the interruption of the mains voltage does not have an instant effect on the output of the regulator 19. During a time lapse, determined by the energy storage capacity of the regulator 19, the voltage VA remains held constant at the output of the regulator 19, allowing the device 1 to maintain the output voltage VB at a logic 1 potential on the $\overline{\text{RESET}}$ input of the microprocessor 3 for as long as the voltage VA is constant. The delay between the interruption caused by the mains absence detector and the setting of the $\overline{\text{RESET}}$ to 0 is therefore as large as possible, since it is equal to the delay between the action of the mains absence detector and the start of the lowering of the supply voltage VA of the microprocessor. Now, it is important that the delay between the interruption caused by the mains absence detector and the setting of the $\overline{\text{RESET}}$ to 0 is as long as possible, since it is this delay which is used for executing a program for saving the instruction which is being executed in the microprocessor 3 by executing an input-output instruction which empties the contents of the registers of the microprocessor onto the input-output bus IO to be taken to an external storage unit which is not shown.

CLAIMS

1. Device (1) for halting the running of programs being executed in a microprocessor (3) provided with an initialising $\overline{\text{RESET}}$ input and with a supply earth prior to the discontinuance of the supply voltage of the microprocessor (3), of the type comprising a differentiating circuit (4) connected by way of diversion between a supply line VA of the microprocessor (3) and the supply earth of the microprocessor and a current amplifier (5) coupled between the differentiating circuit and the $\overline{\text{RESET}}$ input of the microprocessor (3), characterised in that it comprises:

- a capacitor (13) connected on the one hand in parallel between the $\overline{\text{RESET}}$ input and the supply earth of the microprocessor (3) and on the other hand in series between the supply line VA of the microprocessor (3) and the supply earth through a resistor (12) in order to initialise the microprocessor (3) at the time the supply voltage decreases,

- and in that the differentiating circuit (4) comprises means (14 and 10) in order to control the current amplifier in order to rapidly discharge the capacitor (13) when the supply voltage begins to diminish.

2. Device according to Claim 1, characterised in that the current amplifier (5) is constituted by a transistor (11) placed between the $\overline{\text{RESET}}$ input and the supply earth and controlled at its base by the output of the differentiating circuit.

3. Device according to Claim 2, characterised in that the output of the current amplifier (5) is connected to the common ends of a resistor (12) and of a capacitor (13) connected in series between the supply line VA and earth, the non-common end of the capacitor (13) being connected to the earth of the power supply (2).

4. Device according to Claim 3, characterised in that the differentiating circuit (4) comprises a resistor (6) and a capacitor (7) connected in series with the

terminals of the power supply (2) of the microprocessor (3), the ends common to the capacitor and to the resistor being connected to the emitter of a transistor connected between the ends common to the capacitor (7) and to the resistor (6) and the base of the amplifying transistor (11).

5. Device according to Claim 4, characterised in that the value of the capacitor (7) of the differentiating circuit (4) and the value of the capacitor (13) connected between the $\overline{\text{RESET}}$ output and earth bear the following relationship to each other $\frac{\beta . C_2}{C_3} \gg 10$

wherein β represents the current gain of the current amplifier (5), C_2 denotes the capacity of the capacitor (7) of the differentiating circuit (4) and C_3 denotes the capacity of the capacitor (13) connected to the output of the current amplifier.

6. Device according to Claim 5, characterised in that the current gain is obtained by means of two transistors coupled together as a Darlington pair.

7. Use of the device according to Claim 1 for producing a device for saving the instructions of programs being executed in a microprocessor (3) at the time of mains voltage supply failures, the saving device comprising a mains current absence detector (21) connected between the interrupt control terminal INT of the microprocessor (3) and the mains supply lead of the power supply (2).