ABSTRACT

DATA OUTPUT APPARATUS AND SEMICONDUCTOR APPARATUS INCLUDING THE DATA OUTPUT APPARATUS

A semiconductor apparatus includes a memory controller and data storage configured to input and output data in synchronization with a clock signal provided from the memory controller. The data storage includes a memory cell array and a data output apparatus configure to output read data from the memory cell array by sensing a logic level of the read data during a low-level period of a first clock, which is an inverted signal of a divided clock of the clock signal, and a low-level period of a second clock, the second clock having a set phase delay amount from the divided clock.

FIG. 7