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ABSTRACT

A METHOD OF FABRICATING A GATE DIELECTRIC LAYER WITH REDUCED GATE TUNNELLING CURRENT AND REDUCED BORON PENETRATION

A method of forming a silicon nitride - silicon dioxide, composite gate dielectric layer, offering reduced risk of boron penetration from an overlying boron doped polysilicon gate structure, has been developed. A porous, silicon rich silicon nitride layer is first deposited on a semiconductor substrate, allowing a subsequent thermal oxidation procedure to grow a thin silicon dioxide layer on the semiconductor substrate, underlying the porous, silicon rich silicon nitride layer. A two step anneal procedure is then employed with a first step performed in a nitrogen containing ambient to densify the porous, silicon rich silicon nitride layer, while a second step of the anneal procedure, performed in an inert ambient at a high temperature, reduces the foxed charge at the silicon dioxide - semiconductor interface.

FIGURE 4