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ENHANCED BUS ARBITER UTILIZING VARIABLE PRIORITY AND FAIRNESS

ABSTRACT

A bus arbiter (312) for a computer system having a bus (130) for connection to a plurality of bus devices (118, 131-134) where each bus device (118, 131-134) requests control of bus (130) by use of a bus request signal. The bus arbiter (312) contains logic which incorporates a fairness scheme for controlling and prioritizing the bus request signals based on a predetermined priority of each bus device (118, 131-134) and each bus device's prior access within a fairness cycle. Each device's prior access is tracked by bits in a data register (314) and is determined by whether or not the device (118, 131-134) actually received or sent information over the bus (130) and not by a simple granting of access which could result in a retry signal.

FIG 3

