CLAIMS

1. An electroplating method comprising:

plating a metal material into at least one opening on a patterned substrate, wherein at least a portion of the metal material is characterized by a nanotwin crystal structure; and

polishing an exposed surface of the metal material in the opening to reduce an average surface roughness of the exposed surface to less than or equal to 1 nm, wherein the polished exposed surface comprises at least a portion of the metal material characterized by the nanotwin crystal structure.

2. The electroplating method of claim 1, wherein the metal material characterized by the nanotwin crystal structure is nanotwin copper.

3. The electroplating method of claim 2, wherein the metal material comprises at least a second metal selected from the group consisting of gallium, silver, gold, and platinum.

4. The electroplating method of claim 1, wherein the exposed surface of the metal material is polished with chemical mechanical polishing.

5. The electroplating method of claim 1, wherein the exposed surface of the metal material is further polished with electropolishing.

6. The electroplating method of claim 1, wherein the polishing of the exposed surface of the metal material is performed in an oxygen-free environment, and wherein the polishing removes one or more metal oxides from the exposed surface of the metal material.

7. The electroplating method of claim 1, wherein the metal material comprises a first portion in contact with a bottom surface of the opening that is free of the nanotwin crystal structure and a second portion in contact with the polished exposed surface that comprises the nanotwin crystal structure.

8. The electroplating method of claim 7, wherein the patterned substrate further comprises a barrier layer positioned between the first portion and the second portion of the metal material in the opening.

9. An electroplating method comprising:

plating a first portion of a metal material on a bottom portion of at least one opening on a patterned substrate, wherein the first portion of the metal material is substantially free of nanotwin crystal structures;

forming a barrier layer on the first portion of the metal material; and

plating a second portion of the metal material on the barrier layer, wherein the second portion of the metal material is characterized by a nanotwin crystal structure.

10. The electroplating method of claim 9, wherein the first portion of the metal material is greater than or equal to 50 wt.% of a total amount of the metal material in the opening.

11. The electroplating method of claim 9, wherein the metal material is copper.

12. The electroplating method of claim 11, wherein the second portion of the metal material comprises at least a second metal selected from the group consisting of gallium, silver, gold, and platinum.

13. The electroplating method of claim 9, wherein the barrier layer comprises a metal that is not included in the second portion of the metal material.

14. The electroplating method of claim 9, wherein the method further comprises polishing an exposed surface of the second portion of the metal material in the opening to reduce an average surface roughness of the exposed surface to less than or equal to 1 nm.

15. An integrated circuit device structure comprising:

a patterned substrate comprising at least one opening, wherein the opening includes a top portion and bottom surface; and

a metal-containing material filling at least the top portion of the opening, wherein the metal-containing material comprises an exposed surface having an average surface roughness of the exposed surface less than or equal to 1 nm, and wherein the metal-containing material is characterized by a nanotwin crystal structure.

16. The integrated circuit device structure of claim 15, wherein the patterned substrate further comprises a barrier layer positioned between the metal-containing material

filling the top portion of the opening and a second portion of the metal-containing material in contact with the bottom surface of the opening.

17. The integrated circuit device structure of claim 16, wherein the second portion of the metal-containing material is free of the nanotwin crystal structure.

18. The integrated circuit device structure of claim 15, wherein the metal-containing material comprises copper.

19. The integrated circuit device structure of claim 18, wherein the metal-containing material in the top portion of the opening comprises at least a second metal selected from the group consisting of gallium, silver, gold, and platinum.

20. The integrated circuit device structure of claim 15, wherein the opening is characterized by an aspect ratio greater than or equal to 1:1.