

PROCESS FOR MANUFACTURE OF MOS GATED
DEVICE WITH SELF ALIGNED CELLS

ABSTRACT OF THE DISCLOSURE

An MOS-gated power semiconductor device is formed by a process in which a self-aligned device cell is formed without any critical alignments. A sidewall spacer is used to mask the etching of a depression in the silicon to reduce the number of critical alignment steps. A optional selectively formed metal connects the polysilicon layer to the P+ and N+ diffusion regions. The sidewall spacer, in combination with the selectively formed metal, prevents impurities from diffusing to the parasitic DMOS channels and inverting them to cause leakage. A termination structure may also be formed by this process.

Fig. 3