WHAT IS CLAIMED IS:

1. An image processing device configured to compress first image data, the image processing device comprising:

an encoding circuit configured to compress the first image data into second image data comprising prediction data and residual data, compress the second image data into third image data by performing entropy encoding on the second image data,

the encoding circuit further configured to generate a header representing a fixed compression ratio of the third image data, and store the third image data along with the header in a memory device as compressed first image data when the image processing device is set to a lossless compression mode.

2. The image processing device of claim 1, further comprising:

an intellectual property (IP) core directly connected to the encoding circuit; and

a data bus directly connected to the IP core and the memory device,

wherein the encoding circuit receives the first image data directly from the IP core, the encoding circuit transmits the compressed first image data directly to the IP core, and the IP core transmits the compressed first image data across the data bus for storage in the memory device.

3. The image processing device of claim 1, further comprising:

an intellectual property (IP) core; and

a data bus directly connected to the IP core, the encoding circuit, and the memory device,

wherein the encoding circuit receives the first image data indirectly from the IP core through the data bus and the encoding circuit transmits the compressed first image data indirectly to the memory device through the data bus.

4. The image processing device of claim 1, further comprising:

an intellectual property (IP) core; and

a data bus directly connected to the IP core and the encoding circuit,

wherein the encoding circuit receives the first image data indirectly from the IP core through the data bus and the encoding circuit transmits the compressed first image data directly to the memory device.

5. The image processing device of any one of claims 1 to 4, wherein the header includes an index corresponding to one compression ratio range among a plurality of available compression ratio ranges, and the compression ratio of the third image data fits within the one compression range.

6. The image processing device of any one of claims 1 to 5, wherein the encoding circuit adjusts a size of the compressed first image data to a size of a data access unit of the memory device.

7. The image processing device of any one of claims 1 to 6, wherein the compressed first image data further includes at least one entropy encoding value used in the entropy encoding.

8. The image processing device of claim 7, wherein the entropy encoding comprises quantizing the second image data using at least one quantization parameter (QP) and performing entropy encoding on a result of the quantizing.

9. The image processing device of claim 8, wherein the compressed first image data further includes the at least one QP.

10. The image processing device of any one of claims 1 to 9, wherein the encoding circuit comprises a mode selection circuit configured to receive information indicating that a compression mode is one of i) a concatenation mode, ii) a partial concatenation mode, and iii) a separation mode,

wherein during the concatenation mode, the encoding circuit compresses the first image data by combining luma data, first chroma data, and second chroma data into first combined data and compressing the first combined data,

wherein during the partial concatenation mode, the encoding circuit compresses the first image data by compressing the luma data, combining the first chroma data and the second chroma data into second combined data and compressing the second combined data, and

wherein during the separation mode, the encoding circuit compresses the first image data by separately compressing the luma data, the first chroma data, and the second chroma data.

11. An image processing device configured to compress first image data, the image processing device comprising:

an encoding circuit comprising:

a mode selection circuit configured to determine whether a first mode is set to a lossless compression mode or a lossy compression mode based on a received signal;

a first logic circuit configured to compress the first image data into second image data comprising prediction data and residual data;

a second logic circuit configured to quantize the second image data using at least one quantization parameter (QP);

a third logic circuit configured to compress the second image data into third image data and storing the third image data in a memory device as compressed first image data by performing entropy encoding on one of i) an output of the first logic circuit by generating a header representing a fixed compression ratio of the third image data, and storing the header in the memory device when the first mode is set to the lossless compression mode and ii) an output of the second logic circuit when the first mode is set to the lossy compression mode.

12. The image processing device of claim 11, further comprising:

an intellectual property (IP) core directly connected to the encoding circuit; and

a data bus directly connected to the IP core and the memory device,

wherein the encoding circuit receives the first image data directly from the IP core, the encoding circuit transmits the compressed first image data generated based on an output of the third logic circuit directly to the IP core, and the IP core transmits the compressed first image data across the data bus for storage in the memory device.

13. The image processing device of claim 11, further comprising:

an intellectual property (IP) core; and

a data bus directly connected to the IP core, the encoding circuit, and the memory device,

wherein the encoding circuit receives the first image data indirectly from the IP core through the data bus and the encoding circuit transmits the compressed first image data generated based on an output of the third logic circuit indirectly to the memory device through the data bus.

14. The image processing device of claim 11, further comprising:

an intellectual property (IP) core; and

a data bus directly connected to the IP core and the encoding circuit,

wherein the encoding circuit receives the first image data indirectly from the IP core through the data bus and the encoding circuit transmits the compressed first image data generated based on an output of the third logic circuit directly to the memory device.

15. The image processing device of any one of claims 11 to 14, wherein the header includes an index corresponding to one compression ratio range among a plurality of available compression ratio ranges, and the compression ratio fits within the one compression range.

16. The image processing device of any one of claims 11 to 15, wherein encoding circuit adjusts a size of the first compressed data to a size of a data access unit of the memory device.

17. The image processing device of any one of claims 11 to 16, wherein the compressed first image data further includes at least one entropy encoding value using the entropy encoding.

18. The image processing device of any one of claims 11 to 17, wherein the compressed first image data further includes the at least one QP when the first mode is set to the lossy compression mode.

19. The image processing device of any one of claims 11 to 18, wherein the mode selection circuit is configured to determine whether a second mode is set to one of i) a concatenation mode, ii) a partial concatenation mode, and iii) a separation mode,

wherein during the concatenation mode, the first logic circuit compresses the first image data by combining luma data, first chroma data, and second chroma data into first combined data and compressing the first combined data,

wherein during the partial concatenation mode, the first logic circuit compresses the first image data by compressing the luma data, combining the first chroma data and the second chroma data into second combined data and compressing the second combined data, and

wherein during the separation mode, the first logic circuit compresses the first image data by separately compressing the luma data, the first chroma data, and the second chroma data.