

PULSE SIGNAL GENERATORS

This invention relates to pulse signal generators.

It has been previously proposed to employ, for generating pulses of variable duration, a pulse signal generator in which a plurality of stages of delay gates are connected in series with one another so as to transmit an input signal with a time delay. Such a pulse signal generator may, for example, comprise, as shown in block diagram form in Figure 1 of the accompanying drawings, a delay circuit having a plurality of stages of delay gates Ga_1 to Ga_n , a plurality of multiplexers M_1 to M_{n-1} , and a latch circuit 1. In such a circuit configuration including 2^n delay gates Ga , $2^n - 1$ multiplexers are required. In the illustrated example, the delay circuit is composed of eight delay gates Ga_1 to Ga_8 , seven multiplexers M_1 to M_7 and a latch circuit 1 for latching a digital signal of 3 bits (D_0 to D_2). An input pulse signal and a delayed pulse signal obtained from the delay circuit are supplied to a set input terminal S and a reset input terminal R, respectively, of an R-S flip-flop 2 so as to generate a pulse signal having a predetermined pulse duration.

In a delay circuit of the construction shown in Figure 1, control signals S_0 to S_6 outputted from the latch circuit 1 serve to control the operations of the multiplexers M_1 to M_7 , respectively, whereby each of the signals received from input terminals IN, INB is delayed by a predetermined time. Consequently, the disadvantage arises that fixed delay amounts are accumulated and increased due to passage of the signals through the n multiplexers between the individual delay gates and an output terminal Q_1 , thereby prolonging the minimum formable pulse duration. In addition, there is another disadvantage in that delay errors caused by the multiplexers M_1 to M_7 are integrated in accordance with an increase in the number of multiplexers through which the signals pass, hence impairing the monotony of the delay characteristic.

In an attempt to solve the above problems, that is to enhance both the precision and monotony of the pulse duration and also to reduce the minimum formable pulse duration, differential amplifiers DA_1 , DA_2 , DA_3 each comprising a pair of transistors Tr can be connected to delay gates Gb1, Gb2, Gb3, respectively, as shown in Figure 2 of the accompanying drawings, and outputs of the pairs of

transistors Tr constituting the differential amplifiers can be supplied to a cascode amplifier 10, thereby switching on or off a pair of differential amplifier transistors 10a, 10b which constitute the cascode amplifier 10. In this construction, resistors R_1 , R_2 are
 5 connected to output terminals of the transistors 10a, 10b, respectively.

Accordingly, when switching circuits SW_1 , SW_2 , SW_3 ... are selectively actuated in accordance with a given delay condition to operate one of the differential amplifiers DA_1 , DA_2 , DA_3 , then
 10 signals OUT and OUTB, delayed by a predetermined time with respect to the input signals with extremely high precision, can be obtained from output terminals of the pair of differential amplifier transistors 10a, 10b.

However, when the input signal is delayed in this manner, the
 15 problem arises that jitter is caused in an operation performed at superhigh speed

Consider an exemplary case where the output of the delay gate Gb_n in the circuit configuration of Figure 2 is selected when the switching circuit SW_n is at a high level ("H").

20 In this state, if the terminal IN is switched from a low level ("L") to a high level ("H") in response to a pulse fed to the input terminal, then the base voltage of a transistor Tr_{11} of the differential amplifier DA_1 is switched from "L" to "H" after elapsing of the propagation delay time of the delay gate Gb_1 . Subsequently, the base
 25 voltages of transistors Tr_{21} , Tr_{31} Tr_{n1} of the differential amplifiers DA_2 , DA_3 are switched sequentially from "L" to "H". The base voltages of other transistors Tr_{12} , Tr_{22} Tr_{n2} of the differential amplifiers DA_1 , DA_2 ... are switched from "H" to "L".

At the time of state transition of each transistor Tr , a current
 30 for charging the capacitance of the base-emitter junction of the transistor Tr flows in the amplifier 10 cascode-connected to the transistor Tr , so that such current appears as noise in the output signals OUT and OUTB.

For example, when the output is transmitted to the cascode
 35 amplifier 10 after the switching circuit SW_n is selected upon passage of the input pulse through the n stages of delay circuits, if another pulse is fed to the input terminal then that other pulse flows in the

resistors R_1 , R_2 via the parasitic capacitance of each transistor Tr. Consequently, noise is induced at points C and CB and is thereby superposed on the output waveform of the cascode amplifier 10. As a result, the amplitude of the signal obtained from the output terminals
 5 OUT and OUTB becomes different from a predetermined value, which brings about the disadvantage of causing jitter.

The reason for the occurrence of such jitter will now be described with reference to waveform charts shown in Figures 3 to 5 of the accompanying drawings. Figures 3 and 4 show voltage waveforms
 10 obtained at points A, AB, C and CB in Figure 2 when signals are fed to the input terminals IN and INB, Figure 4 being an enlarged view of a portion of Figure 3 proximate to 800 ps. In Figures 3 and 4, I represents a first voltage scale indicative of the potentials at the points A and AB, and II represents a second voltage scale indicative of
 15 the potentials at the points C and CB.

As can be seen from Figures 3 and 4, when an input signal is applied, noise N having an amplitude of 12 mV or so is generated in the vicinity of 800 ps. As shown in a waveform chart represented in Figure
 20 5 of the accompanying drawings, due to the generation of such noise the amplitude of the signal becomes different from its normal value so as consequently to cause a time delay t at the position of inversion of the signal polarity, thus inducing jitter.

In the pulse signal generator of Figure 2, to enable the pulse duration to be changed, the plurality of stages of delay gates are
 25 connected in series with one another to delay the input signal by a predetermined time. As shown in block diagram form in Figure 2, one delay circuit comprises a plurality of stages of delay gates Gb_1 to Gb_{n+1} , differential connection circuits DA_1 to DA_{n+1} for transmitting the signal through the delay gates Gb_1 to Gb_{n+1} at a predetermined timing to
 30 the output circuit 10, and switching circuits SW_1 to SW_{n+1} for selectively operating the delay gates Gb_1 to Gb_{n+1} .

A required number, e.g. 128, of such delay circuits are connected in series with one another, and the switching circuits SW_1 , SW_2 , SW_3 SW_{n+1} are selectively actuated in accordance with a given delay
 35 condition to operate one of the differential amplifiers DA_1 , DA_2 , DA_3 DA_{n+1} , whereby the input signal (supplied via an input buffer circuit) is delayed by a predetermined time with extremely high

precision, and the delayed signal is transmitted from the output terminals OUT and OUTB of the output circuit 10.

The required number of delay circuits are connected in series with one another via delay-circuit connecting wires. In such a series arrangement of the delay circuits, it is possible to connect all of the delay circuits in a row if the connection joints are small in number. However, in the aforementioned exemplary case where a multiplicity (e.g. 128) of the delay circuits are arranged in a pattern layout on a semiconductor chip, a linear or straight arrangement is generally not achievable. Therefore, when forming a series connection of multiple delay circuits, it is customary to employ a pattern layout such as is illustrated in Figure 6 of the accompanying drawings, where the delay circuits are arranged in a plurality (e.g. four) of 32 stages.

In such an arrangement divided into a plurality of stages, the series connections present no problem. However, the delay-circuit connecting wire 22 at each turned portion 23, that is where a delay circuit at the end of one stage is connected to a delay circuit at an end of another stage, is longer than that in any other portion. Consequently, the wiring capacitance at each turned portion 23 becomes far greater than that at the other (straight) portions, bringing about the disadvantage that the delay time linearity is deteriorated at the turned portions 23.

According to the invention there is provided a pulse signal generator comprising:

a plurality of stages of delay gates connected in series with one another for delaying input signals supplied to input terminals;

first differential connection circuits interposed between the respective delay gate stages so as to transmit, at a predetermined timing, the signals passed through the delay gates;

first and second input lines for supplying output signals of the first differential connection circuits to a cascode amplifier; and

second differential connection circuits each comprising a pair of transistors arranged to be supplied with the same input signals as those fed to a pair of transistors of a corresponding said first differential connection circuit, each second differential connection circuit being connected to said first and second input lines in such a manner that outputs of the transistors thereof become inverse in polarity to outputs of the transistors of the corresponding first

differential connection circuit.

According to a preferred feature of the invention, the first and second input lines of the pulse signal generator are connected to a cascode amplifier which comprises:

5 a pair of differentially connected transistors for converting a current change into a voltage change;

a pair of signal output transistors connected to collectors of the differentially connected transistors respectively so as to receive a voltage signal produced by the differentially connected transistors;

10 a pair of differential amplifier transistors having bases connected to emitters of the signal output transistors respectively; and

a load connected to collectors of the differential amplifier transistors so that the collector voltage thereof is changed in accordance with the base voltage thereof;

15 the bases of the signal output transistors being connected to the collectors of the differential amplifier transistors respectively.

An embodiment of the invention described in detail below provides a pulse signal generator which is capable of reducing a minimum formable pulse duration while suppressing the occurrence of jitter, even in superhigh-speed operation.

The invention will now be further described, by way of illustrative and non-limiting example, with reference to the accompanying drawings, in which:

25 Figure 1 is a circuit block diagram of a first previously proposed pulse signal generator;

Figure 2 is a circuit block diagram of a second previously proposed pulse signal generator;

30 Figure 3 is a waveform timing chart of voltages produced in the pulse signal generator shown in Figure 2;

Figure 4 is a waveform timing chart showing characteristic portions of the waveform timing chart of Figure 3;

Figure 5 is a waveform chart for use in explaining a time delay caused by noise;

35 Figure 6 illustrates a pattern of arrangement of delay circuits as shown in Figure 2;

Figure 7 is a circuit diagram of principal components of a pulse signal generator according to an embodiment of the invention;

Figure 8 is a waveform timing chart of voltages produced when a pulse input is supplied to the pulse signal generator shown in Figure 7;

Figure 9 is a waveform timing chart showing characteristic portions of the chart of Figure 8;

Figure 10 is a circuit diagram of a cascode circuit which can be used as a cascode amplifier in the pulse signal generator of Figure 7; and

Figure 11 graphically shows an operating characteristic of the cascode circuit of Figure 10.

A pulse signal generator according to an embodiment of the invention will now be described with reference to Figure 7, which is a circuit diagram thereof. This embodiment is concerned with a circuit for outputting a delayed signal.

As shown in Figure 7, the pulse signal generator comprises a plurality of delay gates Gc_1 , Gc_2 , Gc_3 connected in series with one another. A first differential connection circuit and a second differential connection circuit are interposed between each adjacent pair of the delay gates Gc_1 , Gc_2 , Gc_3 Each pair of first and second differential connection circuits can be the same as the others, whereby only the pair designated 31 (the first differential connection circuit) and 32 (the second differential connection circuit) in Figure 7 will be described.

The first differential connection circuit 31 comprises a pair of transistors 31a, 31b connected in a mutually differential manner, and a switching transistor 31c turned on at a predetermined timing selected by a selector 33. The circuit 31 serves to transmit input signals to output terminals OUT and OUTB via a cascode amplifier 34.

The second differential connection circuit 32, which serves to reduce the noise described above, comprises a pair of transistors Tr32a, Tr32b connected similarly to the first differential connection circuit 31, and a transistor Tr32c which corresponds to the switching transistor Tr31c and is connected to the pair of transistors Tr32a, Tr32b. The transistor Tr32c is kept in an off-state with its emitter and base being connected directly to each other.

The first and second differential connection circuits 31, 32 are connected to input lines Q and QB of the cascode amplifier 34 in such

a manner that outputs of the transistors Tr31a, Tr31b and outputs of the transistors Tr32a, Tr32b obtained from their respective collectors become of mutually inverse polarity.

5 With regard to the transistors Tr31a and Tr32a, whose bases are connected to each other, the transistor Tr31a is connected to the input line Q while the transistor Tr32a is connected to the input line QB. As for the other transistors Tr31b and Tr32b corresponding to each other, the transistor Tr31b is connected to the input line QB while the transistor Tr32b is connected to the input line Q.

10 In the pulse signal generator according to this embodiment, the mutually corresponding ones of the transistors of the first and second differential connection circuits 31, 32 are connected to the input lines Q and QB of the cascode amplifier 34 in such a manner that the respective outputs become of inverse polarity with respect to each other, as mentioned above, so that when pulse signals are fed to input
15 terminals IN and INB, the transistors with base voltages switched from a low level ("L") to a high level ("H") and the same number of the transistors with base voltages switched from "H" to "L" are both connected to one input line. It therefore follows that, at the time of
20 state transition of the transistors, the charge/discharge currents relative to the junction capacitances of the transistors cancel each other out. Accordingly, as graphically shown in a characteristic diagram represented in Figure 8 and an enlarged characteristic diagram represented in Figure 9, none of the above-mentioned noise N appears at
25 the output terminal CB. Consequently, it becomes possible completely to prevent the disadvantage of the occurrence of the delay time Δt described above with reference to Figure 5, thus suppressing the generation of jitter even in the event of input of a random pulse to a superhigh-speed delay line.

30 In the embodiment of the invention described above, the delay gates for delaying an input signal are connected in series with one another in an arrangement to form a plurality of stages. A first differential connection circuit is interposed between adjacent delay gates so as to transmit the signal, and a second differential
35 connection circuit having the same construction as the first differential connection circuit is also interposed between the adjacent delay gates in such a manner that, at the time of state transition of the transistors, charge/discharge currents for the junction

capacitances of the transistors cancel each other out. Thus, the entire time required for forming an output pulse signal, from the beginning to the end, can be controlled with remarkably high precision, with the further advantage of greatly enhancing the accuracy of the pulse duration. In addition, it also becomes possible to prevent superposition on the main signal of noise derived from charge/discharge currents for the capacitance of the base-collector junction of each transistor constituting the first differential connection circuit. Consequently no jitter is induced by input of any random pulse signal.

Figure 10 is a circuit block diagram of a cascode circuit 37. The cascode circuit 37 is effective in greatly improving characteristics when applied to the cascode amplifier 34 of the embodiment of the invention shown in Figure 7.

In the cascode circuit 37, as shown in Figure 10, the base of a transistor Tr65 is connected to a junction of the emitter of a transistor Tr61 and the collector of a transistor Tr63.

The base of a transistor Tr66 is connected to a junction of the emitter of a transistor Tr62 and the collector of a transistor Tr64. Furthermore, n diodes DI_1 to DI_n are connected as a load to the collector of the transistor Tr65 (Tr66), and the base of the transistor Tr61 (Tr62) is connected to the junction of the collector of the transistor Tr65 (Tr66) and the diodes DI_1 to DI_n . The emitters of the transistors Tr65, Tr66 are connected to each other and are further connected via a constant current source to a power source V_{EE} .

When the transistor Tr63 is switched on, it follows that the collector current of the transistor Tr63 is increased. Therefore, the potential difference between the emitter and the base of the transistor Tr61 needs to be sufficiently large. Accordingly, if the base voltage of the transistor Tr61 were fixed, the emitter voltage would need to be lowered. In contrast therewith, the present cascode circuit 37 is so formed that the emitters of the transistors Tr65 and Tr66 are connected to each other and, when the emitter voltage of the transistor Tr61 is about to be lowered, the base voltage of the transistor Tr65 is lowered instead, whereby its collector voltage is increased. More specifically, the base-emitter voltage of the transistor Tr65 is lowered at the above timing so as consequently to reduce the current flowing in the transistor Tr65. Therefore, the current flowing in the

n diodes Di_1 to Di_n connected to the collector of the transistor Tr65 is also reduced to lower the forward voltage V_f , whereby the base voltage of the transistor Tr61 is increased in proportion thereto. As a result, the base-emitter potential difference of the transistor Tr61 is increased quickly so as immediately to cause a flow of an operating current therein.

Since the emitter of the transistor Tr61 is given a sufficiently great capacitance, it has been the case heretofore that a long time is required for lowering the emitter voltage. The base has no capacitance and therefore the base voltage is increased immediately in accordance with a fall of the emitter voltage of the transistor Tr61. Accordingly, in the cascode circuit 37, the transistor Tr61 can be turned on very much faster than in a previously proposed circuit in which the base voltage is fixed, thereby realising quicker transmission of the signal despite the existence of any large stray capacitance.

The above operation will now be described more specifically with the use of mathematical expressions. The transistors Tr63, Tr64 are switched on and off by input voltages V_{IN} and V_{INB} . When the voltage V_{IN} applied to the transistor Tr63 is at a high level ("H"), the base-emitter voltage V_{BE1} of the transistor Tr61 is varied by a value of $kT/q \cdot I_n (I_0 + 2I)/I_0$ under the following conditions:

$$V_A = V - \Delta V \quad \dots (1), \text{ and}$$

$$V_B = V + \Delta V \quad \dots (2).$$

Consequently,

$$\begin{aligned} & [\{ V + \Delta V - (V - \Delta V) \} / 2r_e \times nre + \Delta V] \\ & = kT/q \cdot I_n (I_0 + 2I)/I_0 \quad \dots (3). \end{aligned}$$

Therefore,

$$\Delta V = 1/(n + 1) \cdot kT/q \cdot I_n (I_0 + 2I)/I_0 \quad \dots (4).$$

Since the transistors Tr63 and Tr64 are switched on and off, the emitter voltages thereof are each varied by a value of $1/(n + 1) \cdot kT/q \cdot I_n (I_0 + 2I)/I_0$.

Accordingly, in the cascode circuit 37, a desired result is

attained by charging and discharging by the amount Q as set out in Equation (5) below, despite the existence of any parasitic capacitance such as wiring capacitance in the collectors of the transistors Tr63 and Tr64:

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$$Q = C.kT/q.l_n (I_0 + 2I)/I_0 \quad \dots (5).$$

Thus, it becomes possible to achieve a large enhancement in the operating speed.

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Similarly to the description given above with regard to the transistor Tr63, the same operation can be performed relative to the transistor Tr64 as well. If the transistor Tr64 is switched off, a current I_0 alone comes to flow in the collector of the transistor Tr62. Therefore, the emitter voltage of the transistor Tr62 is urged to rise.

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When the emitter voltage of the transistor Tr62 is about to be increased, the base voltage of the transistor Tr66 is raised to increase the base-emitter voltage of the transistor Tr66, whereby the current flowing in the transistor Tr66 is also increased so as consequently to raise the voltage applied to the diodes Di_1 to Di_n . As a result, the base voltage of the transistor Tr62 is lowered to bring about a fast reduction of the base-emitter voltage V_{BE2} of the transistor Tr62. Therefore, the transistor Tr62 is switched off quickly, and thus delay due to stray capacitance can be greatly diminished on the side relative to the transistors Tr62 and Tr64.

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Figure 11 is a characteristic diagram graphically showing a comparison between the operation of the cascode circuit 37 shown in Figure 10 and the operation of a previously proposed cascode circuit. In this diagram, a broken-line curve A represents the characteristic obtained when one diode D is connected in the cascode circuit 37, and a solid-line curve B represents the characteristic of the previously proposed cascode circuit.

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As is apparent from Figure 11, the voltage change gradient in the cascode circuit 37 can be rendered sharper than that in the previously proposed circuit so as consequently to ensure with certainty a reduction of the signal delay caused by stray capacitance.

Attention is directed to our copending Application No. 9412110.0 (Publication No. GB-A-) which was divided

out of the present application and which includes claims directed to the cascode circuit described herein with reference to Figures 10 and 11.

CLAIMS

1. A pulse signal generator comprising:
 - a plurality of stages of delay gates connected in series with one
 - 5 another for delaying input signals supplied to input terminals;
 - first differential connection circuits interposed between the respective delay gate stages so as to transmit, at a predetermined timing, the signals passed through the delay gates;
 - first and second input lines for supplying output signals of the
 - 10 first differential connection circuits to a cascode amplifier; and
 - second differential connection circuits each comprising a pair of transistors arranged to be supplied with the same input signals as those fed to a pair of transistors of a corresponding said first differential connection circuit, each second differential connection
 - 15 circuit being connected to said first and second input lines in such a manner that outputs of the transistors thereof become inverse in polarity to outputs of the transistors of the corresponding first differential connection circuit.
- 20 2. A pulse signal generator substantially as herein described with reference to Figures 7 to 9 of the accompanying drawings.
3. A pulse signal generator according to claim 1 or claim 2, wherein the first and second input lines are connected to a cascode amplifier
- 25 which comprises:
 - a pair of differentially connected transistors for converting a current change into a voltage change;
 - a pair of signal output transistors connected to collectors of the differentially connected transistors respectively so as to receive
 - 30 a voltage signal produced by the differentially connected transistors;
 - a pair of differential amplifier transistors having bases connected to emitters of the signal output transistors respectively; and
 - a load connected to collectors of the differential amplifier
 - 35 transistors so that the collector voltage thereof is changed in accordance with the base voltage thereof;
 - the bases of the signal output transistors being connected to the collectors of the differential amplifier transistors respectively.



4. A pulse signal generator according to claim 1, wherein the first and second input lines are connected to a cascode amplifier substantially as herein described with reference to Figures 10 and 11 of the accompanying drawings.

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5. A pulse signal generator according to claim 2 which incorporates a cascode amplifier substantially as herein described with reference to Figures 10 and 11 of the accompanying drawings.