Description

This invention relates to integrated semiconductor memory circuits and more particularly to a memory with a very high density of cells, each of which employs means for storing a binary digit of information in a trench or groove.

Integrated semiconductor memory circuits, particularly those employing cells which include essentially a storage capacitor and a switch have achieved high memory cell densities. One of the simplest circuits for providing a small dynamic memory cell is described in commonly assigned U. S. Patent No. 3,387,286, filed July 14, 1967, by R. H. Dennard. Each cell employs a storage capacitor and a field effect transistor acting as a switch to selectively connect the capacitor to a bit/sense line.

In also commonly assigned U. S. Patents Nos. 3,811,076 by W. M. Smith, and 3,841,926 by R. R. Garnache and W. M. Smith, both filed on January 2, 1973, there is disclosed a one device field effect transistor memory cell of the type described in the hereinabove identified Dennard patent which utilizes a layer of doped polysilicon and an N+ diffusion region in a P type conductivity semiconductor substrate separated by a dielectric medium disposed on the surface of the semiconductor substrate for forming the storage capacitor of the well. The polysilicon layer extends beyond the storage capacitor to act as a field shield between adjacent cells by applying a negative bias or fixed negative potential to the polysilicon layer. The N+ diffusion region of the storage capacitor is formed by using a doped segment of an insulating layer disposed on the surface of the semiconductor substrate and outdiffusing the dopant into the substrate.

Although the cells described hereinabove do provide memories having a high density of cells in a planar or two dimensional arrangement, yet each cell does require a significant given area of semiconductor substrate surface. To reduce the size of the given surface area for each cell, structures have been made wherein a semiconductor device or a cell is formed in a three dimensional arrangement. In commonly assigned U. S. Patent 4,295,924, filed on December 17, 1979 by R. R. Garnache and D. M. Kenney, there is disclosed a semiconductor device located within a groove or trench with a self-aligned conductive layer formed on a wall of the trench either directly or on a supporting insulating layer as an element of the device. A memory cell formed in a groove or trench is described in commonly assigned U. S. Patent No. 4,335,450, filed on January 30, 1980, by D. R. Thomas, wherein there is disclosed a cell having a transistor disposed on a sidewall of a groove or trench with the storage node disposed below the transistor. Also U. S. Patent 4,327,476, filed on November 28, 1980, describes a vertical cell having the storage capacitor in a well or trench.

Patent Cooperation Treaty (PCT) Publication No. WO 81/03241, dated November 12, 1981, discloses a one device memory cell structure wherein the storage capacitor is disposed in a trench with the switching device and bit/sense line located at the surface of the substrate.

Furthermore, commonly assigned U. S. Patent No. 4,462,040, filed on March 30, 1980, by I. T. Ho and J. Riseman, discloses a one device dynamic random access memory utilizing a trench having vertical sidewalls with the storage capacitor and the transfer device located within the trench, and U. S. Patents No. 4,271,418, filed on October 29, 1979, and 4,225,945, filed on June 6, 1977, and commonly assigned U. S. Patent Application having Serial No. 793,401, filed on October 31, 1985, by D. M. Kenney, teach a one device memory cell formed in a goove or trench with the storage node located at the bottom of the trench, the bit/sense line at the top of this structure and the transfer device on the sidewall of the trench.

Such a memory is described in EP-A-0 135 942. This semiconductor memory uses the side wall part of a recess dug in a Si substrate as the major part of the electrode surface of a capacitor, whereby the electrode area is enlarged without enlarging a plane area. Thus, a capacitor having a large capacitance can be attained without increasing the breakdown of an insulator film ascribable to the thinning of the insulator film. In addition, a vertical switching transistor is formed on the Si substrate, whereby the Si substrate can be entirely utilized for the formation of the capacitor.

DE-A-3 525 418 discloses a further such memory device on a semiconductor substrate having a trench containing a storage capacitor at the bottom of the trench and a transfer transistor on the sidewalls of the trench. The control gate of the transistor forms part of a word line which extends along the trench above the capacitor. A bit/sense line is arranged on the surface of the substrate orthogonal to the word line.

European patent application EP-A-0 198 590 discloses a further similar semiconductor memory device. This document falls under Article 54(3) EPC and is therefore not relevant to the question of inventive step.

U. S. Patent 4,222,062, filed on May 4, 1976, discloses a memory cell structure wherein a switching device is formed near the bottom of a trench with the bit line and storage capacitor located at a wall of the trench.

Commonly assigned U. S. Patent Application having Serial No. 858,787, filed on May 2, 1986, by B. F. Fitzgerald, K. Y. Nguyen and S. V. Nguyen, describes a dynamic memory cell wherein the

switching device is located at the bottom of the trench, with the storage capacitor and the bit/sense line being formed along opposite sidewalls of the trench.

None of the hereinabove cited prior art discloses a memory cell having a semiconductor substrate surface area of less than four lithographic squares.

It is an object of this invention to provide a semiconductor memory or a memory array or a dynamic memory with a cell or storage means which occupies, along with necessary isolation means, only two lithographic squares of the surface of a semiconductor substrate, wherein one lithographic square is defined by the intersection of two lithographic lines, each line being of any given width, e. g., less than a micron, as used in forming elements of devices in integrated semiconductor circuits.

A semiconductor memory array that solves the aforementioned problems is defined in claim 1.

In a particular embodiment of the present invention, a dynamic random access memory is provided which includes a semiconductor substrate having a major surface and a trench formed therein, first and second spaced apart storage capacitors disposed along one sidewall of the trench, first and second spaced apart bit/sense diffusion regions disposed along the surface of the substrate and a word line disposed along the one sidewall of the trench between the first and second capacitors and the first and second bit/sense diffusion regions. The memory may further include first and second bit/sense lines connected to the first and second bit/sense diffusion regions, respectively, and arranged orthogonal to the direction of the trench. Furthermore, the memory may include similarly arranged elements on the opposite sidewall of the trench connected to the first and second bit/sense lines.

The foregoing and other objects, features and advantages of the invention will be apparent from the following and more particular description of the preferred embodiments of the invention, as illustrated in the accompanying drawings.

Fig. 1
is a circuit diagram of a dynamic one device memory cell indicating the principal elements thereof,

Fig. 2
is a sectional view taken through line 2-2 of Fig. 3 of two dynamic cells of the structure of the present invention,

Fig. 3
is a plan view of two cells of the present invention disposed on opposite sidewalls of a trench,

Fig. 4
is a plan view of a 2x2 array of cells, each cell being of the type illustrated in Figs. 2 and 3,

Figs. 5 and 6
are sectional views of the array illustrated in Fig. 4 taken through lines 5-5 and 6-6, respectively, and

Figs. 7, 8, 9 and 10
are sectional views of the cell illustrated in Figs. 2 and 3 taken during successive steps of the process of making the cells.

Referring to the drawings in more detail, there is shown in Fig. 1 a basic circuit diagram of a well known one device dynamic memory cell 10 which includes a field effect transistor 12 having a gate 14, a storage capacitor 16 having a conductive plate 18 and a storage node 20, and a bit/sense line 22. As is known, to store a binary digit in the storage capacitor 16, a high or low voltage is applied to the bit/sense line 22 and the transistor 12 is turned on to charge the storage node 20 if a high voltage was applied to the bit/sense line 22, indicating the presence of, say, a 1 digit, otherwise the storage node 20 remains uncharged, indicating the presence of a stored 0 digit. To read information from the storage capacitor 16, the bit/sense line 22 is charged to a high voltage and the transistor 12 is turned on. If the bit/sense line 22 is discharged, a sense amplifier (not shown) connected to the bit/sense line 22 will indicate the presence of a 0 digit in the storage capacitor 16. If the bit/sense line 22 remains charged, the storage capacitor 16 is storing a 1 digit.

In accordance with the teachings of this invention, a novel vertical structure of the memory circuit of Fig. 1 is illustrated in Figs. 2 and 3, wherein Fig. 3 is a plan view of the structure and Fig. 2 is a sectional view taken through line 2-2 of Fig. 3. As shown in Figs. 2 and 3, two dynamic memory cells 10A and 10B are disposed on opposite sidewalls within a trench 24 formed in a semiconductor substrate 26, preferably made of silicon and having a P- conductivity. Cell 10A includes the field effect transistor 12, the storage capacitor 16 and the bit/sense line 22, preferably made of metal such as copper-doped aluminum, with transistor 12 and the capacitor 16 being located within the trench 24 on a first sidewall thereof and the bit/sense line 22 being formed on the surface of the substrate 26 in contact with an N+ diffusion region 28 disposed at the surface of the substrate 26, serving as the drain of the transistor 12. The transistor 12 includes the gate 14, which is preferably made of P-doped polysilicon, tungsten silicide (WSi_2) or titanium silicide ($TiSi_2$), or a combination of the polysilicon and a silicide, or of copper-doped aluminum, separated from the first sidewall of the trench 24 by a thin insulating layer 30, preferably a triple insulating layer made of silicon dioxide, silicon nitride and silicon dioxide, or a dual layer made of silicon

dioxide and silicon nitride. The storage capacitor 16 includes the storage node 20 made in the form of an N+ diffusion region disposed along the first sidewall of the trench 24 and the conductive plate 18, which may be made of P-doped polysilicon including boron, separated from the node or N+ diffusion region 20 by an insulating layer 32, preferably also a dual or triple insulating layer made of silicon dioxide and silicon nitride.

A thick layer of insulation 34 is disposed between the bottom of the trench 24 and the conductive plate 18, a layer of insulation 36 is preferably grown, to a thickness of about 100 nm (1000 angstroms), as silicon dioxide on the polysilcon plate 18 so as to isolate the gate 14 from the polysilicon plate 18, and insulating material 38, preferably polyimide or a reflowable glass, such as borophosphosilicate glass, is disposed between the the silicon dioxide layer 36 and the bit/sense line 22.

The second dynamic memory cell 10B is also located within the trench 24 with its field effect transistor 12′ and storage capacitor 16′ being disposed on the second or opposite sidewall of the trench 24, with the bit/sense line 22 being common to both cells 10A and 10B. The second transistor 12′ includes the gate 14′, which is preferably made of the same material as gate 14, separated from the second sidewall of the trench 24 by the thin insulating layer 30. The storage capacitor 16′ includes the storage node 20′ also made in the form of an N+ diffusion region disposed along the second sidewall of the trench 24 within the semiconductor substrate 26 and the conductive plate 18 separated from the N+ diffusion region 20′ by the insulating layer 32. An N+ diffusion region 28′, serving as the drain of the field effect transistor 12′, is connected to the common bit/sense line 22.

Gates 14 and 14′ are portions of first and second word lines 40 and 40′, respectively, which extend in a vertical direction along the longitudinal axis of the trench 24 and orthogonal to the direction of the bit/sense line 22, as indicated in Fig. 3 of the drawings.

It can be seen from Figs. 2 and 3 that two very compact one device dynamic memory cells 10A and 10B are provided on opposite sidewalls of a trench 24 isolated from each other, and from any adjacent cells, by the thick insulation layer 34, wherein all elements of the two cells 10A and 10B are located within a trench 24 except for the bit/sense line 22. The trench 24 may be made as deep and as wide as necessary to provide a storage capacitor of desired size and a transistor of desired switching characteristics. In one arrangement of the structure of the present invention, the depth of the trench 24 is preferably 7 micrometres, with a width of one micron, and the width of the channel of the transistors 12 and 12′ being one micron, with the length of the channel being equal to one micron. The layer of insulation 30 forming the gate insulating medium of the transistors 12 and 12′ has a thickness of about 18 nanometers, with the thickness of the silicon dioxide layers each being 5 nanometers and the thickness of the silicon nitride layer being 8 nanometers. The thickness of the dielectric layer 32 of the storage capacitor 16 is preferably 13 nanometers, e. g., 4 nanometers of silicon dioxide, 7 nanometers of silicon nitride and 2 nanometers of silicon dioxide. The layers of insulation 30 and 32 may also be made of the same continuous materials and having the same thicknesses. The thick layer of insulation 34 preferably has a thickness of 200 nanometers. The N+ diffusion regions 20 and 20′ each extend into the substrate 26 about 150 nanometers from their respective sidewalls of the trench 24. With a spacing between adjacent cells of an array of cells along the word line direction equal to one micron or less and along the bit/sense line direction, which is orthogonal to that of the word line direction, equal to one micron or less, the size of one cell at the surface of the semiconductor substrate may be made equal to 2 square microns or less, which is produced when the lithographic line width is equal to one micron or less. Furthermore, the capacitance of each of the storage capacitors 16 and 16′ versus the capacitance of the bit/sense line 22, assuming 64 cells per bit/sense line, provides a very desirable transfer ratio of at least 20%.

Fig. 4 is a plan view of an array of cells, each cell being of the type illustrated in Figs. 2 and 3 of the drawings, wherein like reference characters refer to similar elements, with two cells 10A and 10B aligned in the horizontal direction along the first bit/sense line 22 and two cells 10C and 10D aligned in the horizontal direction along a second bit/sense line 22′. The cells 10A and 10C are also aligned in the vertical direction along word line 40 and the cells 10B and 10D are aligned in the vertical direction along word line 40′. As is known, each of the word lines 40 and 40′ is connected to word decoder and driver circuits 42 for selective actuation and each of the bit/sense lines 22 and 22′ may be connected to known bit line decoder, precharge and sense amplifier circuits 44.

Fig. 5 is a sectional view of Fig. 4 taken through line 5-5 thereof and Fig. 6 is a sectional view of Fig. 4 taken through line 6-6 thereof to more clearly show the details of the elements of the cells 10A, 10B, 10C and 10D of the array.

By referring to Figs. 4 and 5, wherein Fig. 5 is a sectional view taken orthogonally through the trench 24 in an isolation region between storage nodes of the cells, it can be readily seen that the thick insulating layer 34 is formed along the

sidewalls and the bottom of the trench 24 and on the upper surface of the semiconductor substrate 26. The conductive plate 18 is disposed at the bottom of the trench 24 on the thick insulating layer 34, and the word lines 40 and 40′ are disposed above the plate 18 on opposite sidewalls of the trench 24, separated from the semiconductor substrate 26 by the thick insulation layer 34 and from the conductive plate 18 by the insulation layer 36. The polyimide or BPSG 38 completes the filling of the trench 24.

By referring to Figs. 4 and 6 of the drawings, wherein Fig. 6 is a sectional view taken parallel to a sidewall of the trench 24 and through the storage nodes 20′ and the drain regions 28′, it can be seen that the first bit/sense line 22 contacts, in a self-aligned manner, the drain region 28′ of the cell 10B with its storage node 20′ spaced from the drain region 28′ by the length of the channel of transistor 12′, and the second bit/sense line 22′ contacts the drain region 28′ of the cell 10D with its storage node 20′ spaced from the drain region 28′ of the cell 10D by the length of the channel of its transistor 12′.

As is known, to write into or read from a random access memory array as shown in Fig. 4, word line decoder and driver circuits 42 and bit line decoder, precharge and sense amplifier circuits 44 of any known type may be used to select any one or more of the cells 10A, 10B, 10C and 10D. Furthermore, it should be understood that the trench 24 may contain hundreds of memory cells along each of the two sidewalls thereof to which the word lines 40 and 40′ may be connected and that hundreds of similar spaced apart trenches may be arranged parallel to the trench 24 containing similar memory cells to which the bit/sense lines 22 and 22′ may be connected. The trenches 24 may be spaced apart by one lithographic line, i. e., by as short a distance as one micrometre or less.

Any known process may be used to make the memory cells of the present invention. In one particular process, boron ions with an energy of 10 Mev are implanted through a major surface of the semiconductor substrate 26 to produce a concentration of 1E17 to a depth of about 7 micrometers. The deep trenches 24 about 7 micrometers deep, in the silicon substrate 26 shown in Figs 2, 3, 4 and 5 of the drawings may be formed by known reactive ion etching techniques, preferably with the use of any known lithographicly defined silicon dioxide masking layer. After the trenches 24 are formed, the thick insulating layer 34 may be deposited within the trenches 24 and on the surface of the semiconductor substrate 26. The thick insulating layer 34 is removed, preferably by any known multilayer or multilevel photoresist (MLR) process, including a non-erodable layer, from selected segments of the sidewalls of the trenches 24 where the field effect transistors 12 and 12′ and the storage capacitors 16 and 16′ are to be formed, as well as along the upper surface of the substrate 26 for the formation of the drain regions 28 and 28′ of the transistors 12 and 12′ as indicated in Fig. 7 of the drawings. The thick insulation layer 34 is retained at the bottom of the trenches 24 by blocking the segment of the thick insulation layer 34 at the bottom of the trenches 34 with a layer of photoresist 46, left in place by terminating the MLR reactive ion etch photoresist etching before reaching the trench bottom, as also indicated in Fig. 7 of the drawings. As can be seen in Fig. 8 of the drawings, in the isolation regions between cells along the sidewalls of the trenches, the layer of photoresist 46 prevents the removal of the thick insulation layer 34 during a wet etch process which removes the unwanted segments of the thick insulation layer 34. If desired, the thick insulation layer 34 may be a dual layer made of grown silicon dioxide and deposited silicon nitride.

After the thick insulation layer 34 has been appropriately etched, a layer of doped silicon dioxide 48, about 20 nanometers thick, is deposited conformally along the sidewalls of the trenches 24. Again with the use of a layer of photoresist (not shown), portions of the doped insulation layer 48 at the upper regions of the trenches 24 are removed, as indicated in Fig. 9 at the cell region and in Fig. 10 at the isolation region of the drawings. More specifically, a preferred processing sequence includes coating the structure with a planarizing photoresist which fills the trenches 24, reactively ion etching the planarized photoresist to the desired level in the trenches 24, and removing the doped silicon dioxide 48 from the upper portion of the trenches 24 using dilute buffered hydrogen fluoride. With the layer 48 appropriately etched, by using known drive-in techniques, the dopant, which is preferably arsenic, in the doped insulation layer 48 is driven into the sidewalls of the trenches 24 to form the N+ diffusion regions or storage nodes 20 and 20′, as also indicated in Fig. 9 of the drawings. As can be seen in Fig. 10 of the drawings, since the thick insulation layer 34 is retained on the sidewalls of the trenches 24 between the cells, the arsenic is blocked from entering into the semiconductor substrate 26 at those locations. After drive-in, any appropriate wet etchant, such as the dilute buffered hydrogen fluoride, may be used to remove the remaining segments of the doped insulation layer 48.

With the storage nodes 20 and 20′ formed in the sidewalls of the trenches 24, the gate dielectric layer 30 and the storage capacitor dielectric layer 32 may be formed simultaneously by first growing a layer of silicon dioxide and then depositing a

layer of silicon nitride, followed by oxidation of the nitrides to form 2-4 nanometers of silicon dioxide on top of the nitride. The conductive plate 18 is formed by depositing doped polysilicon into the trenches 24 and planarizing the polysilicon at the surface of the substrate 26. After the polysilicon is planarized, the polysilicon is removed from the upper portion of the trenches 24 by appropriate etching until the upper surface thereof is located below the upper edge of the storage nodes 20 and 20', as indicated in Fig. 2 of the drawings. The exposed surface of the polysilicon plate 18 is now oxidized to form the layer of silicon dioxide 36, which may be, e. g., 100 nm (1000 angstroms) thick. The gates 14 and 14' of the transistors 12 and 12', respectively, may then be formed by depositing another layer of doped polysilicon over the structure and reactively ion etching the polysilicon until the gates 14 and 14' take on the shape indicated in Fig. 2 of the drawings. If preferred, the polysilicon layer may be followed by the deposition of a layer of tungsten silicide or titanium silicide and then reactively ion etched to provide a dual layered gate structure which is more conductive than a gate which is made of only doped polysilicon. By using reactive ion etching techniques, the silicon dioxide and silicon nitride layers 30, 32 can be removed from all horizontal surfaces, particularly from the drain regions 28 and 28' at the surface of the semiconductor substrate 26. The N+ drain regions 28 and 28' are formed by implanting arsenic at 50 KEV and a dose of 1E15 per centimeter square into the exposed surface of the sub strate 26. If desired, copper-doped aluminum may also be used to make the gates 14 and 14', but only after the N+ drain regions 28 and 28' have been formed. The remaining portion of the trenches 24 is filled with insulating material 38 such as polyimide or a reflowable glass, e. g., borophosphosilicate glass, and planarized at the major surface of the semiconductor substrate 26. To form the bit/sense lines 22 and 22', a layer of, preferably, copper-doped aluminum is deposited over the surface of the structure and appropriately etched into parallel lines, as more clearly indicated in Fig.4 of the drawings.

It should be understood that the gate dielectric layer 30 may differ from the capacitor dielectric layer 32 as to composition or thickness, by forming the gate dielec tric layer 30 after forming the conductive plate 18.

It can be readily seen in accordance with the teachings of this invention that an improved memory cell has been provided in a vertical structure within a semiconductor substrate requiring a very small cell substrate surface area, i.e., only two lithography squares, not known in the prior art, by forming within a trench or groove the storage means, the switching means and the word line of the cell, with the bit/sense line disposed on the surface of the semiconductor substrate and arranged orthogonal with respect to the the direction of the word line or trench.

Claims

1. Dynamic random access memory array comprising a semiconductor substrate having a major surface and a trench disposed therein;
first and-second spaced apart storage capacitors comprising diffused regions disposed along a first sidewall of said trench and a conductive plate disposed within said trench and insulated from said diffused regions; first and second spaced apart bit/sense diffusion regions disposed at the surface of said substrate;
a first word line disposed along said first sidewall between said first and second storage capacitors and said first and second bit/sense diffusion regions, respectively, and insulated from said first sidewall and said conductive plate;
the first and second bit/sense lines (22, 22') connected to said first and second bit/sense diffusion regions, respectively, and arranged orthogonal to the direction of said trench, wherein said trench has a second sidewall opposing said first sidewall and further including:
third and forth spaced apart storage capacitors comprising diffused regions disposed along said second sidewall and said conductive plate disposed within said trench and insulated from said diffused regions; third and fourth spaced apart bit/sense diffusion regions disposed at the surface of said substrate, and
a second word line disposed along said second sidewall between said third and fourth capacitors and said third and fourth bit/sense diffusion regions, respectively, and insulated from said second sidewall and said conductive plate,
said first and second bit/sense lines being connected to said third and fourth bit/sense diffusion regions, respectively;
and further including an insulating medium disposed between said first and second word lines wherein said insulating medium is polyimide or reflowable glass.

2. Dynamic random access memory array as set forth in claim 1, characterized by
an insulation layer disposed on said conductive plate between said word lines and said conductive plate.

layer of silicon nitride, followed by oxidation of the nitrides to form 2-4 nanometers of silicon dioxide on top of the nitride. The conductive plate 18 is formed by depositing doped polysilicon into the trenches 24 and planarizing the polysilicon at the surface of the substrate 26. After the polysilicon is planarized, the polysilicon is removed from the upper portion of the trenches 24 by appropriate etching until the upper surface thereof is located below the upper edge of the storage nodes 20 and 20′, as indicated in Fig. 2 of the drawings. The exposed surface of the polysilicon plate 18 is now oxidized to form the layer of silicon dioxide 36, which may be, e. g., 100 nm (1000 angstroms) thick. The gates 14 and 14′ of the transistors 12 and 12′, respectively, may then be formed by depositing another layer of doped polysilicon over the structure and reactively ion etching the polysilicon until the gates 14 and 14′ take on the shape indicated in Fig. 2 of the drawings. If preferred, the polysilicon layer may be followed by the deposition of a layer of tungsten silicide or titanium silicide and then reactively ion etched to provide a dual layered gate structure which is more conductive than a gate which is made of only doped polysilicon. By using reactive ion etching techniques, the silicon dioxide and silicon nitride layers 30, 32 can be removed from all horizontal surfaces, particularly from the drain regions 28 and 28′ at the surface of the semiconductor substrate 26. The N+ drain regions 28 and 28′ are formed by implanting arsenic at 50 KEV and a dose of 1E15 per centimeter square into the exposed surface of the sub strate 26. If desired, copper-doped aluminum may also be used to make the gates 14 and 14′, but only after the N+ drain regions 28 and 28′ have been formed. The remaining portion of the trenches 24 is filled with insulating material 38 such as polyimide or a reflowable glass, e. g., borophosphosilicate glass, and planarized at the major surface of the semiconductor substrate 26. To form the bit/sense lines 22 and 22′, a layer of, preferably, copper-doped aluminum is deposited over the surface of the structure and appropriately etched into parallel lines, as more clearly indicated in Fig.4 of the drawings.

It should be understood that the gate dielectric layer 30 may differ from the capacitor dielectric layer 32 as to composition or thickness, by forming the gate dielec tric layer 30 after forming the conductive plate 18.

It can be readily seen in accordance with the teachings of this invention that an improved memory cell has been provided in a vertical structure within a semiconductor substrate requiring a very small cell substrate surface area, i.e., only two lithography squares, not known in the prior art, by forming within a trench or groove the storage means, the switching means and the word line of the cell, with the bit/sense line disposed on the surface of the semiconductor substrate and arranged orthogonal with respect to the the direction of the word line or trench.

Claims

1. Dynamic random access memory array comprising a semiconductor substrate having a major surface and a trench disposed therein;
first and-second spaced apart storage capacitors comprising diffused regions disposed along a first sidewall of said trench and a conductive plate disposed within said trench and insulated from said diffused regions; first and second spaced apart bit/sense diffusion regions disposed at the surface of said substrate;
a first word line disposed along said first sidewall between said first and second storage capacitors and said first and second bit/sense diffusion regions, respectively, and insulated from said first sidewall and said conductive plate;
the first and second bit/sense lines (22, 22') connected to said first and second bit/sense diffusion regions, respectively, and arranged orthogonal to the direction of said trench,
wherein said trench has a second sidewall opposing said first sidewall and further including:
third and forth spaced apart storage capacitors comprising diffused regions disposed along said second sidewall and said conductive plate disposed within said trench and insulated from said diffused regions; third and fourth spaced apart bit/sense diffusion regions disposed at the surface of said substrate, and
a second word line disposed along said second sidewall between said third and fourth capacitors and said third and fourth bit/sense diffusion regions, respectively, and insulated from said second sidewall and said conductive plate,
said first and second bit/sense lines being connected to said third and fourth bit/sense diffusion regions, respectively;
and further including an insulating medium disposed between said first and second word lines wherein said insulating medium is polyimide or reflowable glass.

2. Dynamic random access memory array as set forth in claim 1, characterized by
an insulation layer disposed on said conductive plate between said word lines and said conductive plate.

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3. Dynamic random access memory array as set forth in claims 1 or 2 wherein said conductive plate is made of doped polysilicon and said word lines are made of a silicide.

4. Dynamic random access memory array as set forth in claim 1 wherein said conductive plate is made of doped polysilicon, said word lines are made of doped polysilicon and said bit/sense lines are made of copper-doped aluminum.

5. Dynamic random access memory array as set forth in claim 1, characterized by
a thick layer of insulation disposed on said first sidewall between said first and second storage capacitors and between said first and second bit/sense diffusion regions.

6. Memory as set forth in claim 1 wherein the diffusion regions of said first and second capacitors and the diffusion regions of said third and fourth capacitors are separated by first and second layers of insulation, respectively.

7. Memory as set forth in claim 1 wherein said first and second bit/sense lines include aluminum.

Patentansprüche

1. Matrix von dynamischen Schreiblesespeichern, die folgendes umfaßt:
ein Halbleitersubstrat mit einer Hauptoberfläche und einem darin angebrachten Graben;
erste und zweite getrennt voneinander angeordnete Speicherkondensatoren mit entlang einer ersten Seitenwand des Grabens angeordneten Diffusionsbereichen und einer im Graben und von den Diffusionsbereichen isoliert angeordneten leitenden Platte;
erste und zweite an der Oberfläche des Substrats getrennt voneinander angebrachte Bit/Lesediffusionsbereiche;
eine erste entlang der ersten Seitenwand zwischen den ersten und zweiten Speicherkondensatoren und den ersten und zweiten Bit/Lesediffusionsbereichen und von der ersten Seitenwand und der leitenden Platte isoliert angeordnete Wortleitung;
erste und zweite mit den ersten bzw. zweiten Bit/Lesediffusionsbereichen verbundene und orthogonal zur Richtung des Grabens angeordnete Bit/Leseleitungen (22, 22');
wobei der Graben gegenüber der ersten eine zweite Seitenwand aufweist;
und die weiterhin folgendes umfaßt:
dritte und vierte voneinander getrennte Speicherkondensatoren mit entlang der zweiten Seitenwand angeordneten Diffusionsbereichen und einer im Graben und von den Diffusionsbereichen isoliert angeordneten leitenden Platte;
dritte und vierte an der Oberfläche des Substrats getrennt voneinander angebrachte Bit/Lesediffusionsbereiche;
eine zweite entlang der zweiten Seitenwand zwischen den dritten und vierten Kondensatoren und den dritten und vierten Bit/Lesediffusionsbereichen und von der zweiten Seitenwand und der leitenden Platte isoliert angeordnete Wortleitung, wobei die ersten bzw. zweiten Bit/Leseleitungen mit den dritten bzw. vierten Bit/Lesediffusionsbereichen verbunden sind; und weiterhin
ein zwischen den ersten und zweiten Wortleitungen angebrachtes isolierendes Medium, wobei das isolierende Medium ein Polyimid oder ein aufschmelzbares Glas ist.

2. Matrix von dynamischen Schreiblesespeichern nach Anspruch 1, dadurch gekennzeichnet, daß
eine Isolationsschicht auf der leitenden Platte zwischen den Wortleitungen und der leitenden Platte angebracht ist.

3. Matrix von dynamischen Schreiblesespeichern nach Ansprüchen 1 oder 2, bei der die leitende Platte aus dotiertem Polysilicium und die Wortleitungen aus einem Silicid bestehen.

4. Matrix von dynamischen Schreiblesespeichern nach Anspruch 1, bei der die leitende Platte aus dotiertem Polysilicium, die Wortleitungen aus dotiertem Polysilicium und die Bit/Leseleitungen aus kupferdotiertem Aluminium bestehen.

5. Matrix von dynamischen Schreiblesespeichern nach Anspruch 1, dadurch gekennzeichnet, daß
eine dicke Isolationsschicht auf der ersten Seitenwand zwischen den ersten und zweiten Speicherkondensatoren und zwischen den ersten und zweiten Bit/Lesediffusionsbereichen angebracht ist.

6. Speicher nach Anspruch 1, bei dem die Diffusionsbereiche der ersten und zweiten Kondensatoren und die Diffusionsbereiche der dritten und vierten Kondensatoren durch erste bzw. zweite Isolationsschichten getrennt werden.

7. Speicher nach Anspruch 1, bei dem die ersten und zweiten Bit/Leseleitungen Aluminium ent-

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halten.

Revendications

1. Réseau de mémoire dynamique à accès aléatoire, comprenant un substrat semi-conducteur ayant une surface principale comportant une tranchée ;
   - un premier et un second condensateurs de stockage séparés l'un de l'autre, comprenant des régions diffusées disposées le long d'une première paroi de ladite tranchée et une plaque conductrice située dans ladite tranchée et isolée desdites régions diffusées ; une première et une seconde régions de diffusion de contrôle de bits séparées l'une de l'autre, disposées à la surface dudit substrat ; une première ligne de mots disposée le long de ladite première paroi entre lesdits premier et second condensateurs et lesdites première et seconde diffusions de contrôle de bits respectivement, et isolée de ladite première paroi et de ladite plaque conductrice; les première et seconde lignes de contrôle de bits (22, 22') étant connectées auxdites première et seconde régions de diffusion respectivement et disposées perpendiculairement à la direction de ladite tranchée, laquelle tranchée a une seconde paroi opposée à ladite première paroi et comprenant :
   - un troisième et un quatrième condensateurs de stockage séparés, comprenant des régions de diffusion, disposés le long de ladite seconde paroi et ladite plaque conductrice étant disposée dans ladite tranchée et isolée desdites régions diffusées ; une troisième et une quatrième régions de diffusion de contrôle de bits séparées et placées à la surface dudit substrat et,
   - une seconde ligne de mots disposée le long de ladite seconde paroi entre lesdits troisième et quatrième condensateurs et lesdites troisième et quatrième régions de diffusion de contrôle de bits, et isolée de ladite seconde paroi et de ladite plaque conductrice,
   - lesdites premières et secondes lignes de contrôle de bits étant connectées auxdites troisième et quatrième régions de diffusion de contrôle de bits respectivement ;

   et comprenant en outre un milieu isolant disposé entre lesdites première et seconde lignes de mots, le moyen isolant étant du polyimide ou verre fondu.

2. Réseau de mémoire dynamique à accès aléatoire selon la revendication 1 caractérisé en ce qu'il comporte une couche isolante disposée sur la plaque conductrice entre les lignes de mots et ladite plaque conductrice.

3. Réseau de mémoire dynamique à accès aléatoire selon l'une des revendication 1 ou 2 dans lequel ladite plaque conductrice est faite de polysilicium dopé, et lesdites lignes de mots faites d'une combinaison siliciée.

4. Réseau de mémoire dynamique à accès aléatoire selon la revendication 1 dans lequel ladite plaque conductrice est faite de polysilicium dopé, lesdites lignes de mots sont en polysilicium dopé et lesdites lignes de contrôle de bits en aluminium dopé cuivre, ledit réseau comprenant en outre un milieu isolant entre lesdites première et seconde lignes de mots, ledit milieu isolant étant en polyimide ou en verre fondu.

5. Réseau de mémoire dynamique à accès aléatoire selon la revendication 1 caractérisé en ce qu'il comporte une couche épaisse d'isolation placée sur ladite première paroi entre lesdits premier et second condensateurs de stockage et entre lesdites première et seconde régions de diffusion de contrôle de bits.

6. Mémoire selon la revendication 1 dans laquelle les régions de diffusion desdits premier et second condensateurs et les régions de diffusion desdits troisième et quatrième condensateurs sont séparées par lesdites première et seconde couches d'isolation, respectivement.

7. Mémoire selon la revendication 1 dans laquelle lesdites première et seconde lignes de contrôle de mots comprennent de l'aluminium.

* C L M S *