Description

This invention relates to semiconductor device fabrication and in particular to undercutting etching techniques.

In some structures, for example some types of semiconductor lasers, an active region lies between a substrate and a cap layer. In a single mode, buried heterostructure (BH) laser known for use in optical communications, the active region is provided by a stripe of active material often no more than 5 microns wide and typically of the order of 1 to 2 microns wide. (Additional layers may be included such as a buffer layer on top of the stripe.) The layers for such structures are grown in sequence on a slice and the slice is subjected to additional fabrication procedures in order to define the lateral structure of the active region.

Different fabrication methods are known for achieving a device having a structure of the BH laser type and depending on the method used, and final structure details, the devices will generally have particular characteristics. Some of these methods entail a blind etching step in which material of one layer must be partially removed from beneath another layer, leaving a boundary of material which is overhung. This arises for instance in a constricted mesa laser structure, having an active region which lies under a significantly wider portion of cap layer.

It is beneficial that there should be a little semiconductor material to either side of the active region but that the lateral extent of the cap layer is still significantly greater. The narrow waist at the active region tends to give a laser having relatively low threshold current and high speed response. The semiconductor material at the sides of the active region gives a low degree of carrier recombination at those sides and low shunt currents, and the wider portion of cap layer has been found to give good reliability.

Such a structure can be made from a wafer including substrate, active layer and cap layer by masking part of the cap layer surface, etching away both cap layer and active layer from the unmasked areas, then blind etching the remaining active layer below the cap layer from its exposed sides until only a much narrower active region remains, overhung on both sides by the remaining cap layer. This is achieved by using an etchant that is selective to the material of the active layer. The length of time in the selective etchant determines the width of the defined active region. After the stripe of active material has been defined its exposed sides are covered in semiconductor material.

One of the techniques used for covering the exposed sides of the active region is described by Z L Liau and J N Walpole in Applied Physics Letters Volume 40, No 7, 1 April 1982. In this paper the undercut is formed by blind etching as described above and then the structure is heated in the presence of phosphine so that the sides of the undercut are filled in by mass transport of the material of the cap layer. There are problems associated with controlling the heating stage to ensure the correct flow during mass transport, and so other workers have employed a vapour phase growth step after the undercutting. This type of technique is described in papers by

i) T L Koch et al entitled "Low-Threshold High-Speed 1.55 μm Regrown Buried Heterostructure Lasers" in Proceedings of IEEE 9th International Semiconductor Laser Conference, Brazil 1984, pp 80-81,

ii) T L Koch et al entitled "Low-Threshold High-Speed 1.55 μm Vapour Phase Transported Buried Heterostructure Lasers (VPTBH)" in Electronics Letters 20 (21) October 1984, pp 856,857,

iii) J E Bowers et al entitled "High-frequency Constricted Mesa Lasers" in Applied Physics Letters 47 (2) July 1985, pp 78-80, and

iv) J E Bowers et al entitled "High-frequency Modulation of 1.52 μm Vapour-phase-transported InGaAsP Lasers" in Electronics Letters 21 - (9) 25th April 1985, pp 392,393.

Whichever technique is used these methods still employ the blind etch undercut process which suffers from the disadvantage that there is no direct control over the length of undercut. Various factors including etchants, etching time, temperature, layer thickness and the previous etching stage on the cap layer all contribute to cause fluctuations in the length of undercut and therefore in the defined width of the active region.

The present invention is directed towards providing improved control in fabricating semiconductor structures having undercut semiconductor layers in cross section.

According to a first aspect of the present invention there is provided a technique of fabricating a multi-layer semiconductor structure on a substrate, which technique includes an undercutting step wherein a second layer is undercut by removal of material of a first layer from between the second layer and the substrate, said first and second layers comprising different materials, characterised in that the technique comprises making at least one opening in the first layer through to the substrate; providing the second layer over at least a part of the first layer and into the opening at least as far as the substrate, the portion of the second layer which extends into said opening providing a barrier portion of the second layer; making an access opening in the second layer which is lat-

erally displaced from said barrier portion and exposes said first layer beneath; and selectively removing the first layer by means of the access opening at least partially in the direction of said barrier portion such that said selective removal of the first layer undercuts the second layer, the barrier portion providing a lateral limit to the selective removal of the first layer such that a maximum available degree of undercut is determined by the lateral displacement of the access opening from said barrier portion.

(Although words such as "lower" and "upper" might be used in the present specification, it is for the convenience of description only and should not be taken to indicate any necessary specific orientation unless the context implies otherwise.)

By using a fabrication technique as described above, it is possible to pre-determine at least a limiting position for a boundary in a layer, even in blind etching that layer so as to have the boundary overhung by another layer. Although it may not be necessary to remove all the material of the lower (first) layer which lies between the access opening and the barrier portion of the upper (second) layer, the barrier portion can provide a lateral limit to that removal by protecting the material of the lower layer which lies on the far side of the barrier portion with respect to the access opening, from for instance a selective etchant.

The making of an access opening may not necessarily in practice comprise a separate step in the fabrication technique. The opening may for instance be provided by a boundary in the upper layer which is determined during creation of the upper layer, perhaps by photolithographic masking.

The layers may conveniently be produced by known epitaxial growth techniques such as metal organic vapour phase epitaxy. Each layer and the substrate may in practice comprise sublayers of the same or different materials.

Particularly where the semiconductor structure is a constricted mesa laser structure, the fabrication technique also offers an advantage in the control it can provide over the dimensions of the barrier portion of the upper layer. If the lower layer is an active material layer and the upper layer is the cap layer of such a laser structure, then the barrier portion of the upper layer will constitute the semiconductor material at the sides of the active region in a fabricated device. Because the dimensions of the barrier portion are determined by the step of making the boundary defining opening through the lower layer, those dimensions can be selected and applied by means of a relatively simple, exposed etching process.

(It will be appreciated that during the selective removal of the lower layer with respect to the upper layer, a little material of the upper layer may also be removed, and possibly the dimensions of the barrier portion very slightly reduced. This is because selective etchants are not generally perfectly selective but tend to etch one material at a rate many times faster than the rate at which another material is etched. The effect is not significant however.)

The semiconductor structure may well incorporate semiconductor layers in addition to the lower and upper layers, such as a buffer layer lying between them. This need not affect the creation and use of a barrier portion as described above. It will be understood however that the making of an access opening through the upper layer may not then of itself expose the lower layer at the opening, the access opening having first to be made also in any intervening layer or layers. Such an additional layer may or may not be removed at the same time as the lower layer. For instance, if the additional layer is of the same material as the lower layer except in containing different dopant material, it may well be removed by the same selective etchant as the lower layer.

According to a second aspect of the present invention, there is provided a fabrication technique according to the first aspect as described above, which comprises making two neighbouring openings through the first layer at least as far as the substrate, each of these defining a boundary in the first layer, the second layer extending between and over both of said openings and having two barrier portions which each extend through a respective one of said neighbouring boundary defining openings at least as far as the substrate, making two access openings through the second layer, each lying laterally offset to a different respective side of both boundary defining openings, and selectively removing material of the first layer by means of said two access openings so as to leave of said first layer between said two access openings only the material of the first layer which lies between the two boundary defining openings.

Using fabrication techniques according to the first aspect of the present invention, a semiconductor device structure can be created which comprises a substrate supporting a portion of a first material, which portion has a boundary set back from the edge of the substrate, and an overlying layer of a second material, the overlying layer extending beyond the boundary of the portion of a first material and being undercut substantially up to said boundary, said boundary being concealed by a downwardly extending barrier portion of the overlying layer. The barrier portion is notably an integral part of the overlying layer, being created in the same operation.

It may be preferable in a finished device structure that a layer of dielectric material such as silica

is used to cover all or part of the structure. This dielectric material may fill in the undercut below the overlying layer up to the boundary of the portion of a first material. However, such a finished device structure is still considered to fall within the above description of a semiconductor device structure having an undercut overlying layer when regarded in terms of the semiconductor layers only.

Where the semiconductor structure is a waisted mesa stripe laser structure, the fabrication technique can effectively be applied twice, to create the stripe active region overhung on both sides by a mesa cap layer. The fabrication technique may then comprise the steps of: -

i) creating a wafer having a layer of active material but no cap material;

ii) etching a pair of neighbouring, parallel channels through the layer of active material which are separated by the width of the active region required in the finished laser structure;

iii) depositing a continuous layer of cap material to cover and fill both channels;

iv) etching a mesa in the layer of cap material, which mesa straddles the channels and overhangs on both sides the stripe of active material which lies between the channels; and

v) selectively removing the active material which lies between each edge of the mesa and the nearest channel.

Preferably, the channels should be as narrow as possible, for instance not more than 1 micron wide, so as to minimise shunt currents and stray capacitance in a finished laser structure.

The above can be described as a fabrication technique according to the second aspect of the present invention, wherein said two neighbouring boundary defining openings comprise channels through the first layer to the substrate so as to define, between the channels, a strip in said first layer, and said selective removal of the material of the first layer leaves, of said first layer between the two access openings, only the material of said strip in said first layer which lies between the neighbouring channels.

The word "active" where used in the present specification to describe a material, region or layer, is used in the sense that the material, region or the material of such a layer is capable of lasing action.

Within the context of this specification 'laser structure' includes structures that may be used other than under lasing conditions, eg as a modulator.

The invention will now be described by way of example with reference to the accompanying drawings in which:

Figure 1 is a schematic cross section through a slice or wafer showing the structure of the layers prior to further fabrication.

Figures 2 to 6 are schematic cross sections showing in sequence various stages in the fabrication process, and

Figure 7 is a schematic cross section through a completed laser structure fabricated according to the invention.

The undercutting technique of the invention is described with reference to a buried heterostructure laser. However, it will be realised that a similar technique may be utilized for other structures where a non surface layer requires etching with defined accuracy.

In Figure 1 the starting layers are shown which consist of a substrate 1, active layer 2, and buffer stop layer 3. For optical communication purposes the final laser will require an operating wavelength close to one of the absorption minima of silica fibres, that is with a wavelength in the ranges of 1.25 to 1.35 microns or 1.50 to 1.55 microns. Therefore the structure will preferably comprise an In Ga As P active layer and an InP substrate and it is within this context, with an n-type substrate that the following procedures are described. A 'reverse' structure with p-type substrate and all the other layers of opposite type may be fabricated in an analogous way.

The substrate 1 is a slice of 001 orientation indium phosphide doped n-type to a level in the approximate range 1 to 10, x 10^{18} cm^{-3}. The last 0.1 micron or so of the substrate preferably consists of a separately grown buffer layer also of n-type indium phosphide doped to a level of about 1 x 10^{18} cm^{-3}. The active layer 2 is typically about 0.1 microns thick (the more general range being of the order of 0.05 to 0.4 microns depending upon application) and consists of $In_{0.6}Ga_{0.4}As_{0.88}P_{0.12}$ for 1.5 micron wavelength operation or $In_{0.7}Ga_{0.3}As_{0.64}P_{0.36}$ for 1.3 micron wavelength operation. This active layer is nominally undoped but in practical terms is likely to have a starting n-type level of around 1 x 10^{17} cm^{-3} and after fabrication is completed diffusion from the other layers is likely to turn the active layer p type to a level of about 5 x 10^{17} cm^{-3}. After the active layer is grown the buffer stop layer 3 is deposited which is composed of p-type indium phosphide doped to a level of about 1 x 10^{18} cm^{-3}. This structure is then subjected to photolithographic masking to define four windows through which the buffer layer 3 and active layer 2 are removed as shown in Figure 2 to form channels 4, 5, 6 and 7. A two stage selective etching process is used, for example using 30% hydrochloric acid or a mixture of 4 parts hydrochloric and 1 part (90%) orthophosphoric acid to remove the indium phosphide buffer and 16% iodic acid to remove the In Ga As P. This ensures that the second etch stops (or effectively so as the rate of etching is a factor of 10 or so slower on indium

phosphide) at the substrate surface. The channels 4, 5, 6 and 7 are made as narrow as possible, for example about one micron in width. Channels 5 and 6 are spaced by 1 to 2 microns depending on the desired final width of the active layer which becomes defined in a mesa 8 between channels 5 and 6. It will be realised that although the Figures show sloping sides to the channels the layers 2 and 3 have only a total depth of about 0.2 microns and so the window defined by the photolithography will very closely match the base of the channel. More vertical sides may be achieved, and therefore greater accuracy, by using a dielectric (silica) layer as the mask but for this stage this is usually not necessary. The spacing between channels 4 and 5 and between channels 6 and 7 is not critical.

After the channels have been etched a layer 9 of p-type indium phosphide is grown over the resulting structure, as shown in Figure 3. This layer is typically 1 to 1.5 microns thick doped to a level of 1×10^{18} cm^{-3}. A second masking stage is then performed, which may again be by photolithography only, or a silica mask, itself defined by a photolithography stage, may be used. An etchant selective to indium phosphide (eg 30% HCl) is then used to remove the layer 9 and the buffer layer 3 through the windows of the mask as shown in Figure 4. Then an etchant selective to In Ga As P (eg nitric acid) is used to remove the active layer as shown in Figure 5. Nitric acid is preferred for this stage as it is not particularly selective to crystallographic orientation. It will be realised looking at Figure 5 that the indium phosphide layer 9 is substantially undercut to form cavities 11 by this latter active layer etch, but the extent of the undercutting is defined by the indium phosphide grown in the channels 4, 5, 6 and 7 formed at the first etching stage (Figure 2). Thus once the etchant reaches the indium phoshide filled channels the undercutting stops.

After the undercutting stage a layer 10 of silica (or other dielectric) is grown over the surface to a depth of about 0.3 microns as shown in Figure 6. This silica layer is grown by a vapour phase reaction between silane and oxygen and deposits over the entire surface. The undercut cavities 11 may become filled with silica or some void may remain with only the openings blocked. A window is then opened in the silica in the region above the active layer mesa 8 and a metallisation layer 12 deposited. The device is then completed by metallising the substrate and mounting substrate uppermost on a heat sink. The metallisations comprise a thin layer of titanium followed by a thin layer of gold.

The final laser structure shown in Figure 7 has very low parasitic capacitance and leakage currents due to the comparatively small areas that can give rise to these properties. Both parasitic capacitance and leakage currents depend upon the area of contact between the p-type indium phosphide cap layer 9 and the n-type indium phosphide substrate. In the structure formed in accordance with the invention this is limited to the channel areas 5 and 6, the rest of the structure then being isolated by dielectric.

It will be realised that the device is defined by the active layer mesa 8, the filled channels 5 and 6 and the other parts in the central large mesa 13 of Figure 7. The satellite mesas indicated as 14 are not part of the device as such but aid in providing structural stability and reducing leakage current in the event of pinholes in the dielectric layer 10. Structurally, the laser is mounted substrate uppermost on a heat sink and there is greater stability in mounting the combined surfaces of the mesas 13 and 14 than in mounting the central mesa 13 alone. In the event of pinholes in the dielectric these create much greater leakage currents if they occur on top of the substrate rather than on top of the cap layer 9.

The self stopping undercut technique may be applied to other devices where a buried layer requires etching, examples of devices in which the technique is applicable include electro-optic devices, electro absorption modulators and heterojunction transistors. Other materials than those described may be subjected to selective etching. It is also possible for at least some of the etching to be other than chemical etching; sputtering or ion beam milling may be used which would not be selective but may be used especially for removing the cap layer for example, or reactive ion etching may be used, in this latter case selective etching being achieved by the diffusion contact rather than momentum collision process.

Claims

1. A technique of fabricating a multi-layer semiconductor structure on a substrate (1), which technique includes an undercutting step wherein a second layer (9) is undercut by removal of material of a first layer (2), from between the second layer (9) and the substrate (1), said first and second layers (2, 9) comprising different materials, characterised in that the technique comprises making at least one opening (4, 5, 6, 7) in the first layer (2), through to the substrate (1); providing the second layer (9) over at least a part of the first layer (2) and into the opening (4, 5, 6, 7) at least as far as the substrate (1), the portion of the second layer which extends into said opening providing a barrier portion of the second layer; making an access opening in the second layer (9) which is laterally displaced from said

phosphide) at the substrate surface. The channels 4, 5, 6 and 7 are made as narrow as possible, for example about one micron in width. Channels 5 and 6 are spaced by 1 to 2 microns depending on the desired final width of the active layer which becomes defined in a mesa 8 between channels 5 and 6. It will be realised that although the Figures show sloping sides to the channels the layers 2 and 3 have only a total depth of about 0.2 microns and so the window defined by the photolithography will very closely match the base of the channel. More vertical sides may be achieved, and therefore greater accuracy, by using a dielectric (silica) layer as the mask but for this stage this is usually not necessary. The spacing between channels 4 and 5 and between channels 6 and 7 is not critical.

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barrier portion and exposes said first layer (2) beneath; and selectively removing the first layer (2) by means of the access opening at least partially in the direction of said barrier portion such that said selective removal of the first layer (2) undercuts the second layer (9), the barrier portion providing a lateral limit to the selective removal of the first layer (2) such that a maximum available degree of undercut is determined by the lateral displacement of the access opening from said barrier portion.

2. A technique according to Claim 1 wherein the first layer (2) is entirely removed from the region between the access opening and the barrier portion.

3. A technique according to either one of Claims 1 or 2 wherein the access opening defines a lateral boundary in the second layer (9).

4. A technique according to any one of the preceding claims wherein the semiconductor structure includes at least one additional layer (3) which lies between the first and second layers (2, 9).

5. A technique according to any one of the preceding claims wherein the access opening is provided at least partially by the side of a mesa which overlies the barrier portion of the second layer (9).

6. A technique according to any one of the preceding claims which comprises making two neighbouring openings (5, 6) through the first layer (2) at least as far as the substrate (1), each of these defining a boundary in the first layer (2), the second layer (9) extending between and over both of said openings (5, 6) and having two barrier portions which each extend through a respective one of said neighbouring boundary defining openings (5, 6) at least as far as the substrate (1), making two access openings in the second layer (9), each lying laterally offset to a different respective side of both boundary defining openings (5, 6), and selectively removing material of the first layer (2) by means of said two access openings so as to leave of said first layer between said two access openings only or substantially only the material of the first layer (2) lying between the two boundary defining openings (5, 6).

7. A technique according to Claim 6 wherein the two boundary defining openings (5, 6) define a stripe of material of the first layer (2) which is not more than 5 micrometres wide.

8. A technique according to any one of the preceding claims in which the openings are made by chemical or reactive ion etching.

9. A technique according to any one of the preceding claims in which a dielectric layer (10) is deposited over the access opening or openings in the second layer (9) and over at least part of the surface exposed by the selective removal of the first layer (2).

10. A technique according to any one of claims 1, 3, 4, 5, 7, 8 or 9 in which the first layer (2) is entirely removed from the position of the access opening or openings up to the associated barrier portion, or respective barrier portions, of the second layer (9).

11. A technique according to Claim 6, wherein said two neighbouring openings (5, 6) comprise channels through the first layer (2) to the substrate (1) such that the selective removal of the material of the first layer (2) between the two access openings leaves a strip of the material of the first layer (2) lying between said channels (5, 6).

12. A technique according to Claim 11 for use in making a laser structure, wherein the material of the first layer (2) which lies between the neighbouring channels (5, 6) provides the stripe of active material in a stripe laser structure.

13. A technique according to Claim 12 wherein the distance separating the neighbouring channels (5, 6) is 5 micrometres or less.

Patentansprüche

1. Verfahren zum Herstellen einer Mehrschichten-Halbleiterstruktur auf einem Substrat (1), wobei das Verfahren einen Unterätz-Schritt aufweist, wobei eine zweite Schicht (9) untergeätzt wird durch Entfernen von Material einer ersten Schicht (2) aus dem Bereich zwischen der zweiten Schicht (9) und dem Substrat (1), wobei die erste und zweite Schicht (2, 9) unterschiedliche Materialien aufweisen, dadurch gekennzeichnet, daß das Verfahren die folgenden Schritte aufweist. Herstellen zumindest einer Öffnung (4, 5, 6, 7) in der ersten Schicht (2), und zwar bis zu dem Substrat (1) hindurch, Bereitstellen der zweiten Schicht (9) über zumindest einem Teil der ersten Schicht (2) und in die Öffnung (4, 5, 6, 7) zumindest bis zu

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dem Substrat (1), wobei der Anteil der zweiten Schicht, der sich in die Öffnung erstreckt, einen Grenzanteil der zweiten Schicht bereitstellt, Herstellen einer Zugangsöffnung in der zweiten Schicht (9), welche seitlich verschoben ist von dem Grenzanteil und die erste Schicht (2) exponiert, und selektives Entfernen der ersten Schicht (2) mittels der Zugangsöffnung zumindest teilweise in der Richtung des Grenzanteils, so daß die selektive Entfernung der ersten Schicht (2) die zweite Schicht (9) unterätzt, wobei der Grenzanteil eine seitliche Begrenzung zu der selektiven Entfernung der ersten Schicht (2) bereitstellt, so daß ein maximal zur Verfügung stehender Grad des Unterätzens bestimmt wird durch die seitliche Verschiebung der Zugangsöffnung von dem Grenzanteil.

2. Verfahren nach Anspruch 1, wobei die erste Schicht (2) vollständig entfernt wird von dem Gebiet zwischen der Zugangsöffnung und dem Grenzanteil.

3. Verfahren nach einem der Ansprüche 1 oder 2, wobei die Zugangsöffnung eine seitliche Grenze in der zweiten Schicht (9) definiert.

4. Verfahren nach einem der vorhergehenden Ansprüche, wobei die Halbleiterstruktur zumindest eine zusätzliche Schicht (3) beinhaltet, welche zwischen der ersten und zweiten Schicht (2, 9) liegt.

5. Verfahren nach einem der vorhergehenden Ansprüche, wobei die Zugangsöffnung zumindest teilweise an der Seite der Mesa bereitgestellt ist, welche über dem Grenzanteil der zweiten Schicht (9) liegt.

6. Verfahren nach einem der vorhergehenden Ansprüche, welches die folgenden Schritte aufweist: Herstellen zweier benachbarter Öffnungen (5, 6) durch die erste Schicht (2) zumindest bis zu dem Substrat (1), wobei jede davon eine Grenze in der ersten Schicht (2) definiert, wobei sich die zweite Schicht (9) zwischen und über beide der Öffnungen (5, 6) erstreckt und zwei Grenzanteile hat, die sich jeweils durch eine entsprechende der benachbarten grenzedefinierenden Öffnungen (5, 6) bis zu dem Substrat (1) erstrecken, Herstellen von zwei Zugangsöffnungen in der zweiten Schicht (9), von denen jede seitlich versetzt zu einer unterschiedlichen entsprechenden Seite der grenzedefinierenden Öffnungen (5, 6) liegt, und selektives Entfernen von Material der ersten Schicht (2) mittels der beiden Zugangsöffnungen, so daß man von der ersten Schicht zwischen den beiden Zugangsöffnungen nur oder im wesentlichen nur das Material der ersten Schicht (2) übrig läßt, welches zwischen den beiden grenze-definierenden Öffnungen (5, 6) liegt.

7. Verfahren nach Anspruch 6, wobei die beiden grenze-definierenden Öffnungen (5, 6) einen Streifen Material der ersten Schicht (2) definieren, welcher nicht breiter als 5 Mikrometer ist.

8. Verfahren nach einem der vorhergehenden Ansprüche, bei denen die Öffnungen durch chemisches oder reaktives Ionenätzen hergestellt werden.

9. Verfahren nach einem der vorhergehenden Ansprüche, bei welchem eine dielektrische Schicht (10) über der Zugangsöffnung oder den Zugangsöffnungen in der zweiten Schicht (9) und über zumindest einen Teil der Oberfläche aufgebracht wird, welche durch die selektive Entfernung der ersten Schicht (2) exponiert ist.

10. Verfahren nach einem der Ansprüche 1, 3, 4, 5, 7, 8 oder 9, bei welchem die erste Schicht von der Position der Zugangsöffnung oder den Zugangsöffnungen bis hinauf zu dem zugeordneten Grenzanteil oder entsprechenden Grenzanteilen der zweiten Schicht (9) vollständig entfernt wird.

11. Verfahren nach Anspruch 6, wobei die beiden benachbarten Öffnungen (5, 6) Kanäle aufweisen durch die erste Schicht (2) zu dem Substrat (1), so daß die selektive Entfernung des Material der ersten Schicht (2) zwischen den beiden Zugangsöffnungen einen Streifen Material der ersten Schicht (2) übrig läßt, welcher zwischen den beiden Kanälen (5, 6) liegt.

12. Verfahren nach Anspruch 11 zur Verwendung bei der Herstellung einer Laserstruktur, wobei das Material der ersten Schicht (2), welches zwischen den benachbarten Kanälen (5,6) liegt, den Streifen aktiven Materials in einer Streifenlaserstruktur bereitstellt.

13. Verfahren nach Anspruch 12, wobei der die benachbarten Kanäle (5, 6) trennende Abstand 5 Mikrometer oder weniger ist.

Revendications

1. Une technique de fabrication d'une structure semi-conductrice à couches multiples sur un substrat (1), technique qui inclut une étape de

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gravure sous-jacente dans laquelle une deuxième couche (9) est gravée de manière sous-jacente en enlevant, d'une première couche (2), une matière située entre la deuxième couche (9) et le substrat (1), lesdites première et deuxième couches (2, 9) étant constituées de matières différentes, caractérisée en ce que la technique comprend les étapes consistant à ménager au moins une ouverture (4, 5, 6, 7) dans la première couche (2), à travers le substrat (1); disposer la deuxième couche (9) au-dessus au moins d'une partie de la première couche (2) et dans l'ouverture (4, 5, 6, 7) au moins jusqu'au substrat (1), la partie de la deuxième couche qui s'étend dans ladite ouverture constituant une partie de barrière de la deuxième couche; ménager, dans la deuxième couche (9), une ouverture d'accès qui est décalée latéralement par rapport à ladite partie de barrière et expose ladite première couche (2) située au-dessous; et enlever sélectivement la première couche à l'aide d'une ouverture d'accès au moins partiellement dans la direction de ladite partie de barrière d'une manière telle que ledit enlèvement sélectif de la première couche (2) réalise une gravure sous-jacente à la deuxième couche (9), la partie de barrière constituant une limite latérale à l'enlèvement sélectif de la première couche (2) d'une manière telle qu'un degré maximal disponible de gravure sous-jacente est déterminé par le décalage latéral de l'ouverture d'accès par rapport à ladite partie de barrière.

2. Une technique selon la revendication 1 dans laquelle la première couche (2) est entièrement enlevée de la région comprise entre l'ouverture d'accès et la partie de barrière.

3. Une technique selon l'une des revendications 1 ou 2 dans laquelle l'ouverture d'accès définit une limite latérale dans la deuxième couche (9).

4. Une technique selon l'une quelconque des revendications précédentes dans laquelle la structure semi-conductrice inclut au moins une couche additionnelle (3) qui est située entre la première et la deuxième couches (2, 9).

5. Une technique selon l'une quelconque des revendications précédentes dans laquelle l'ouverture d'accès est constituée au moins partiellement par le côté d'un mésa qui recouvre la partie de barrière de la deuxième couche (9).

6. Une technique selon l'une quelconque des précédentes revendications qui comprend les étapes consistant à ménager deux ouvertures voisines (5, 6) à travers la première couche (2) au moins jusqu'au substrat (1), chacune de celles-ci définissant une limite dans la première couche (2), la deuxième couche (9) s'étendant entre lesdites ouvertures (5, 6) et au-dessus de celles-ci et comportant deux parties de barrière qui s'étendent chacune respectivement à travers l'une des ouvertures voisines (5, 6) définissant une limite au moins jusqu'au substrat (1), ménager, dans la deuxième couche (9), deux ouvertures d'accès décalée chacune latéralement vers un côté respectif différent des deux ouvertures (5, 6) définissant les limites, et enlever sélectivement de la matière de la première couche (2) au moyen desdites deux ouvertures d'accès de façon à ne laisser, de la première couche située entre les deux ouvertures d'accès, que la matière ou sensiblement que la matière de la première couche (2) située entre les deux ouvertures (5, 6) définissant une limite.

7. Une technique selon la revendication 6 dans laquelle les deux ouvertures (5, 6) définissant la limite définissent une bande de matière de la première couche (2) dont la largeur n'est pas supérieure à 5 micromètres.

8. Une technique selon l'une quelconque des revendications précédentes dans laquelle les ouvertures sont réalisées par gravure chimique ou par gravure ionique réactive.

9. Une technique selon l'une quelconque des revendications précédentes dans laquelle une couche diélectrique (10) est déposée au-dessus de l'ouverture ou des ouvertures d'accès de la deuxième couche (9) et au-dessus au moins d'une partie de la surface exposée par l'enlèvement sélectif de la première couche (2).

10. Une technique selon l'une quelconque des revendications 1, 3, 4, 5, 7, 8 ou 9 dans laquelle la première couche (2) est entièrement enlevée de la position de l'ouverture ou des ouvertures d'accès jusqu'à la partie de barrière associée, ou jusqu'aux parties respectives de barrière associées, de la deuxième couche (9).

11. Une technique selon la revendication 6, dans laquelle lesdites deux ouvertures voisines (5, 6) comprennent des canaux à travers la première couche (2) jusqu'au substrat (1) d'une manière telle que l'enlèvement sélectif de la matière de la première couche (2) entre les

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deux ouvertures d'accès laisse une bande de la matière de la première couche (2) située entre lesdits canaux (5, 6).

12. Une technique selon la revendication 11 à utiliser pour fabriquer une structure laser, dans laquelle la matière de la première couche (2) qui est située entre les canaux voisins (5, 6) constitue la bande de matière active d'une structure de laser en bande.

13. Une technique selon la revendication 12 dans laquelle la distance séparant les canaux voisins (5, 6) est de 5 micromètres ou moins.