CLAIMS

What is claimed is:

1. A method of saving power in a wireless device, comprising:

receiving data within a frame at a user equipment (UE);

determining whether all payload packet data has been correctly decoded prior to an end of the frame; and

powering down a receiver component for a portion of a remainder of the frame in response to determining that all payload packet data has been correctly decoded and where a first time period to a next scheduled overhead bit transmission period of a slot in the frame is greater than a second time period corresponding to a warm-up period for the receiver component.

2. The method of claim 1, further comprising maintaining power to the receiver component where the first time period is not greater than the second time period.

3. The method of claim 1, further comprising powering up the receiver component at a first instance prior to an overhead bit transmission period of a slot in the frame, wherein the first instance prior to the overhead bit transmission period corresponds to a warm-up time for the receiver component.

4. The method of claim 3, wherein the powering up occurs once every n slots, and wherein n is a positive integer.

5. The method of claim 1, wherein the UE comprises a plurality of receiver components, further comprising:

powering up a first one of the plurality of receiver components at a first instance prior to an overhead bit transmission period of a slot in the frame, wherein the first instance prior to the overhead bit transmission period corresponds to a start of a warm-up time for the first one of the plurality of receiver components; and

powering up a second one of the plurality of receiver components substantially at a start of the next scheduled overhead bit transmission period.

6. The method of claim 5, wherein powering up the first one of the plurality of receiver components at the first time further comprises powering up a phase-locked loop receiving component.

7. The method of claim 1, wherein the UE comprises a plurality of receiver components, further comprising:

maintaining power to a first one of the plurality of receiver components where a first time period to a next scheduled overhead bit transmission period of a slot in the frame is not greater than a second time period corresponding to a warm-up period for the receiver component;

powering down a second one of the plurality of receiver components where the next scheduled overhead bit transmission period has not yet arrived; and

powering up the second one of the plurality of receiver components substantially at a start of the next scheduled overhead bit transmission period.

8. The method of claim 7, wherein maintaining the power to the first one of the plurality of receiver components further comprises maintaining power to a phase-locked loop receiver component.

9. The method of claim 1, further comprising:

obtaining a threshold dedicated control channel (DCCH) energy value corresponding to a presence of the DCCH, wherein determining whether all payload packet data has been correctly decoded occurs at a time interval prior to an end of the frame;

computing an accumulated DCCH energy value in the frame over the time interval; and

canceling the powering down of the receiver component where the accumulated DCCH energy value is greater than or equal to the threshold DCCH energy value.

10. The method of claim 1, further comprising:

determining that the data comprises first class data having an error detection mechanism and second class data without an error detection mechanism;

wherein determining whether all payload packet data has been correctly decoded further comprises determining that the first class data has been correctly decoded based on the error detection mechanism;

assuming that the second class data has been correctly decoded based on the determining that the first class data has been correctly decoded; and

wherein powering down the receiver component for the portion of the remainder of the frame is in response to the determining that the first class data has been correctly decoded.

11. The method of claim 10, wherein the data comprises data encoded with an Adaptive Multi-Rate (AMR) codec, and wherein the first class data comprises class A data and the second class data comprises class B or class C data.

12. The method of claim 1, wherein determining whether all payload packet data has been correctly decoded further comprises determining that Null and SID data has been correctly decoded.

13. The method of claim 1, wherein the determining comprises passing a Cyclic Redundancy Check.

14. An apparatus for wireless communication, comprising:

means for receiving data within a frame at a user equipment (UE);

means for determining whether all payload packet data has been correctly decoded prior to an end of the frame; and

means for powering down a receiver component for a portion of a remainder of the frame in response to the means for determining making a determination that all payload packet data has been correctly decoded and where a first time period to a next

scheduled overhead bit transmission period of a slot in the frame is greater than a second time period corresponding to a warm-up period for the receiver component.

15. A computer program product for saving power in a wireless device, comprising:

a computer-readable medium executable by a computer and comprising code for:

receiving data within a frame at a user equipment (UE);

determining whether all payload packet data has been correctly decoded prior to an end of the frame; and

powering down a receiver component for a portion of a remainder of the frame in response to determining that all payload packet data has been correctly decoded and where a first time period to a next scheduled overhead bit transmission period of a slot in the frame is greater than a second time period corresponding to a warm-up period for the receiver component.

16. An apparatus for wireless communication, comprising:

at least one processor; and

a memory coupled to the at least one processor, wherein the at least one processor is configured to:

receive data within a frame at a user equipment (UE);

determine whether all payload packet data has been correctly decoded prior to an end of the frame; and

power down a receiver component for a portion of a remainder of the frame in response to determining that all payload packet data has been correctly decoded and where a first time period to a next scheduled overhead bit transmission period of a slot in the frame is greater than a second time period corresponding to a warm-up period for the receiver component.

17. The apparatus of claim 16, wherein the at least one processor is configured to maintain power to the receiver component where the first time period is not greater than the second time period.

18. The apparatus of claim 16, wherein the at least one processor is configured to power up the receiver component at a first instance prior to an overhead bit transmission period of a slot in the frame, wherein the first instance prior to the overhead bit transmission period corresponds to a warm-up time for the receiver component.

19. The apparatus of claim 18, wherein the at least one processor is configured to power up the receiver component once every *n* slots.

20. The apparatus of claim 16, wherein the UE comprises a plurality of receiver components, and wherein the at least one processor is further configured to:

power up a first one of the plurality of receiver components at a first instance prior to an overhead bit transmission period of a slot in the frame, wherein the first instance prior to the overhead bit transmission period corresponds to a start of a warm-up time for the first one of the plurality of receiver components; and

power up a second one of the plurality of receiver components substantially at a start of the next scheduled overhead bit transmission period.

21. The apparatus of claim 16, wherein powering up the first one of the plurality of receiver components at the first time further comprises powering up a phase-locked loop receiving component.

22. The apparatus of claim 16, wherein the UE comprises a plurality of receiver components, and wherein the at least one processor is further configured to:

maintain power to a first one of the plurality of receiver components where a first time period to a next scheduled overhead bit transmission period of a slot in the frame is not greater than a second time period corresponding to a warm-up period for the receiver component;

power down a second one of the plurality of receiver components where the next scheduled overhead bit transmission period has not yet arrived; and

power up the second one of the plurality of receiver components substantially at a start of the next scheduled overhead bit transmission period.

23. The apparatus of claim 22, wherein maintaining the power to the first one of the plurality of receiver components further comprises maintaining power to a phase-locked loop receiver component.

24. The apparatus of claim 16, wherein the at least one processor is further configured to:

obtain a threshold dedicated control channel (DCCH) energy value corresponding to a presence of the DCCH, wherein determining whether all payload packet data has been correctly decoded occurs at a time interval prior to an end of the frame;

compute an accumulated DCCH energy value in the frame over the time interval; and

cancel the powering down of the receiver component where the accumulated DCCH energy value is greater than or equal to the threshold DCCH energy value.

25. The apparatus of claim 16, wherein the at least one processor is further configured to:

determine that the data comprises first class data having an error detection mechanism and second class data without an error detection mechanism;

wherein determining whether all payload packet data has been correctly decoded further comprises determining that the first class data has been correctly decoded based on the error detection mechanism;

assume that the second class data has been correctly decoded based on determining that the first class data has been correctly decoded; and

wherein powering down the receiver component for the portion of the remainder of the frame is in response to the determining that the first class data has been correctly decoded.

26. The apparatus of claim 25, wherein the data comprises data encoded with an Adaptive Multi-Rate (AMR) codec, and wherein the first class data comprises class A data and the second class data comprises class B or class C data.

27. The apparatus of claim 16, wherein determining whether all payload packet data has been correctly decoded further comprises determining that Null and SID data has been correctly decoded.

28. The apparatus of claim 16, wherein the determining comprises passing a Cyclic Redundancy Check.

CLAIMS

1. A method of saving power in a wireless device, comprising:

receiving data within a frame at a user equipment (UE);

determining that the data has been correctly decoded prior to an end of the frame; and

powering down a receiver component of the UE for a portion of a remainder of the frame in response to determining that the data has been correctly decoded and upon a determination that a first time period to a next scheduled overhead bit transmission period of a slot in the frame is greater than a second time period of the slot in the frame corresponding to a warm-up period for the receiver component.

2. The method of claim **1**, further comprising maintaining power to the receiver component where the first time period is not greater than the second time period.

3. The method of claim **1**, further comprising powering up the receiver component at a first instance prior to the next scheduled overhead bit transmission period, wherein the first instance prior to the next scheduled overhead bit transmission period corresponds to a start of the warm-up period.

4. The method of claim **3**, wherein the powering up occurs once every n slots, and wherein n is a positive integer.

5. The method of claim **1**, wherein the UE comprises a plurality of receiver components, the method further comprising:

powering up a first component of the plurality of receiver components at a first instance prior to the next scheduled overhead bit transmission period, wherein the first instance prior to the next scheduled overhead bit transmission period corresponds to a start of a warm-up time for the first component; and

powering up a second component of the plurality of receiver components substantially at a start of the next scheduled overhead bit transmission period.

6. The method of claim **5**, wherein the first component comprises a phase-locked loop receiving component.

7. The method of claim **1**, wherein the UE comprises a plurality of receiver components, the method further comprising:

maintaining power to a first component of the plurality of receiver components where the first time period is not greater than a third time period corresponding to a warm-up period for the first receiver component;

powering down a second component of the plurality of receiver components where the next scheduled overhead bit transmission period has not yet arrived; and

powering up the second component substantially at a start of the next scheduled overhead bit transmission period.

8. The method of claim **7**, wherein the first component comprises a phase-locked loop receiver component.

9. The method of claim **1**, further comprising:

obtaining a threshold dedicated control channel (DCCH) energy value corresponding to a presence of a DCCH, wherein determining that the data has been correctly decoded occurs at a time interval prior to an end of the frame;

computing an accumulated DCCH energy value in the frame over the time interval; and

canceling the powering down of the receiver component where the accumulated DCCH energy value is greater than or equal to the threshold DCCH energy value.

10. The method of claim **1**, further comprising:

determining that the data comprises first class data having an error detection mechanism and second class data without an error detection mechanism;

determining that the first class data has been correctly decoded based on the error detection mechanism; and

assuming that the second class data has been correctly decoded based on determining that the first class data has been correctly decoded, wherein powering down the receiver component for the portion of the remainder of the frame is in response to the determining that the first class data has been correctly decoded.

11. The method of claim **10**, wherein the data comprises data encoded with an Adaptive Multi-Rate (AMR) codec, and wherein the first class data comprises class A data and the second class data comprises class B or class C data.

12. The method of claim **1**, wherein determining that the data has been correctly decoded further comprises determining that Null and SID data has been correctly decoded.

13. The method of claim **1**, wherein determining that the data has been correctly decoded comprises determining that the data has passed a Cyclic Redundancy Check.

14. An apparatus for wireless communication, comprising:

means for receiving data within a frame at a user equipment (UE);

means for determining that the data has been correctly decoded prior to an end of the frame; and

means for powering down a receiver component of the UE for a portion of a remainder of the frame in response to the means for determining making a determination that

the data has been correctly decoded and upon a determination that a first time period to a next scheduled overhead bit transmission period of a slot in the frame is greater than a second time period of the slot in the frame corresponding to a warm-up period for the receiver component.

15. A non-transitory computer-readable medium storing instructions that when executed by a computer cause the computer to:

receive data within a frame at a user equipment (UE);

determine that the data has been correctly decoded prior to an end of the frame; and

power down a receiver component of the UE for a portion of a remainder of the frame in response to determining that the data has been correctly decoded and upon a determination that a first time period to a next scheduled overhead bit transmission period of a slot in the frame is greater than a second time period of the slot in the frame corresponding to a warm-up period for the receiver component.

16. An apparatus for wireless communication, comprising:

at least one processor; and

a memory coupled to the at least one processor, wherein the at least one processor is configured to:

receive data within a frame at a user equipment (UE);

determine that the data has been correctly decoded prior to an end of the frame; and

power down a receiver component of the UE for a portion of a remainder of the frame in response to determining that the data has been correctly decoded and upon a determination that a first time period to a next scheduled overhead bit transmission period of a slot in the frame is greater than a second time period of the

slot in the frame corresponding to a warm-up period for the receiver component.

17. The apparatus of claim **16**, wherein the at least one processor is configured to maintain power to the receiver component where the first time period is not greater than the second time period.

18. The apparatus of claim **16**, wherein the at least one processor is configured to power up the receiver component at a first instance prior to the next scheduled overhead bit transmission period, wherein the first instance prior to the next scheduled overhead bit transmission period corresponds to a start of the warm-up period.

19. The apparatus of claim **18**, wherein the at least one processor is configured to power up the receiver component once every n slots.

20. The apparatus of claim **16**, wherein the UE comprises a plurality of receiver components, and wherein the at least one processor is further configured to:

power up a first component of the plurality of receiver components at a first instance prior to the next scheduled overhead bit transmission period, wherein the first instance prior to the next scheduled overhead bit transmission period corresponds to a start of a warm-up time for the first component; and

power up a second component of the plurality of receiver components substantially at a start of the next scheduled overhead bit transmission period.

21. The apparatus of claim **16**, wherein the first component comprises a phase-locked loop receiving component.

22. The apparatus of claim **16**, wherein the UE comprises a plurality of receiver components, and wherein the at least one processor is further configured to:

maintain power to a first component of the plurality of receiver components where the first time period is not greater than a third time period corresponding to a warm-up period for the first receiver component;

power down a second component of the plurality of receiver components where the next scheduled overhead bit transmission period has not yet arrived; and

power up the second component substantially at a start of the next scheduled overhead bit transmission period.

23. The apparatus of claim **22**, wherein the first component comprises a phase-locked loop receiver component.

24. The apparatus of claim **16**, wherein the at least one processor is further configured to:

obtain a threshold dedicated control channel (DCCH) energy value corresponding to a presence of a DCCH, wherein determining that the data has been correctly decoded occurs at a time interval prior to an end of the frame;

compute an accumulated DCCH energy value in the frame over the time interval; and

cancel the powering down of the receiver component where the accumulated DCCH energy value is greater than or equal to the threshold DCCH energy value.

25. The apparatus of claim **16**, wherein the at least one processor is further configured to:

determine that the data comprises first class data having an error detection mechanism and second class data without an error detection mechanism;

determine that the first class data has been correctly decoded based on the error detection mechanism; and

assume that the second class data has been correctly decoded based on determining that the first class data has been correctly decoded, wherein powering down the receiver component for the portion of the remainder of

the frame is in response to the determining that the first class data has been correctly decoded.

26. The apparatus of claim **25**, wherein the data comprises data encoded with an Adaptive Multi-Rate (AMR) codec, and wherein the first class data comprises class A data and the second class data comprises class B or class C data.

27. The apparatus of claim **16**, wherein determining that thet data has been correctly decoded further comprises determining that Null and SID data has been correctly decoded.

28. The apparatus of claim **16**, wherein determining that the data has been correctly decoded comprises determining that the data has passed a Cyclic Redundancy Check.